

**GOVERNMENT ENGINEERING COLLEGE, THRISSUR**  
**NOTICE INVITING TENDER**

D2/6169/23/GECTCR  
11.08.2023  
**E Tender No. : D2/29/23-24**

**Superscription : Purchase of DSP Trainer kit for  
Electronics Department**

Bidding fee : Rs. 708/-(600 +18%GST )  
EMD required : Rs. 3000/-

Address of the Officer to whom hardcopy is to be sent :  
THE PRINCIPAL,  
GOVERNMENT ENGINEERING COLLEGE,  
RAMAVARMAPURAM, THRISSUR, 680009

**ITEM SPECIFICATION**

Sl.no	Items with specifications	Quantity
	<p><b>TMS320C6748 based DSP Trainer kit with speaker and mic for Codec experiments (Detailed specification attached)</b></p> <p><b><u>Detailed Specifications</u></b> C6748 low-power digital signal processor based on C674x DSP core. It consumes significantly lower power than other members of the TMS320C6000™ platform of DSPs.</p> <p><b>On-Chip Features:</b></p> <ul style="list-style-type: none"><li>• TMS320C674x Fixed/Floating-Point VLIW DSP Core</li><li>• 64 General-Purpose Registers (32 Bit)</li><li>• Six ALU (32-/40-Bit) Functional Units</li><li>• Two Multiply Functional Units</li><li>• Instruction Packing Reduces Code Size</li><li>• All Instructions Conditional</li><li>• Hardware Support for Modulo Loop Operation</li><li>• Real time clock</li></ul> <p><b>On-Chip Memory:</b></p> <p>* Two Level Cache Memory Architecture</p> <ul style="list-style-type: none"><li>• 32K-Byte L1P Program RAM/Cache</li><li>• 32K-Byte L1D Data RAM/Cache</li></ul>	

- 256K-Byte L2 Unified Mapped RAM/Cache

- \* 128K-Byte RAM Shared Memory

**On-Board Features:**

- 2 Meg x 16 Bit x 4 Banks Synchronous DRAM for External Program/Data

- **Codec:**

- Stereo Audio ADC & DAC
- 16/20/24/32-Bit Data Format
- Supports Rates From 8 kHz to 96 kHz
- Programmable Input /Output Analog Gains
- Audio Serial Data Bus Supports I2S, Left/Right-Justified, DSP, and TDM Modes

- **On Board ADC/DAC**

- **ADC:**

- No of ADC input Channels : 2
- Resolution bit: 12
- Sampling rate( max )1Msps
- Analog input range( max ): + 5V
- High speed SPI serial interface

- **DAC:**

- No of DAC outputChannels: 2
- Resolutionbit: 12
- Settling time micro sec ( max )8.5
- Analog output range ( max ): + 5V
- High speed SPI serial interface

- **Extra Features:**

- Provision to connect external JTAG Emulator
- 8 user definable LEDs
- 8 position DIP switch, user definable
- Two 3.5 mm. audio jacks for audio IN and OUT
- Expansion connector for GPIO / Video Add on card

- **JTAG Emulator(XDS100V1):**

Emulation Connect/Disconnect, Read/Write memory, Read registers, Load program, Run, Halt, Step, Software and Hardware Breakpoint support, Real-Time Mode. Support for USB Full Speed (12 Mbits/s)

**List of Deliverables should include:**

**Hardware**

- 6748 Trainer Kit
- USB Cable
- Power Supply +5V Adaptor
- Software CD
- Program & Manual CD

#### **USER MANUAL WITH LIST OF EXPERIMENTS**

- Sampling Theorem
- Impulse Response
- Linear Convolution & Linear Convolution using DFT & IDFT
- Circular Convolution & Circular Convolution using DFT & IDFT
- Auto Correlation
- Cross Correlation
- Solving Difference Equations
- N point DFT and FFT
- Design FIR Filter
- Design IIR Filter
- Noise Removal
- Waveform Generation
- CODEC Loop back, Voice Storing & Retrieval etc.,

Installation, demonstration and and training for the faculty and staff for one day

#### **General conditions**

1. The unit price, all other charges such as delivery, transporting, packing, shipping, loading and unloading charges etc, and GST must be shown separately and should be furnished unambiguously.
2. Payment will be made only after the successful supply, installation and testing.
3. F.O.R: Govt. Engineering College, Thrissur.
4. Agreement: Preliminary Agreement in Rs.220/- Kerala Stamp Paper.
5. Date of opening of tender: In case the proposed date declared as holiday, the tender will be opened on the next working day.
6. After E-tendering the hard copy of all documents should be submitted before the date of opening of the tender to the Principal, Government Engineering College, Thrissur.
7. Items to be supplied at Civil Engineering of Govt. Engineering College, Thrissur.
8. The items should have a minimum guarantee period of one year from the date of installation and successful performance.
9. Installation, successful demonstration and training required.
10. Delivery Period: Immediately after the date of receipt of supply order within two months
11. 5% security deposit along with agreement should be furnished within a month/fortnight from the date of receipt of supply order.
12. Only GST Registered firms should participate in the tender.

13. Bidder shall be responsible for installation / demonstration as applicable and for after sales service during the warranty and thereafter.
14. Installation and demonstration to be arranged by the supplier free of cost and the same is to be done within 15 days of the arrival of the equipment at site.

NB: The Tender procedure will be made as per Rules mentioned in the Revised Store Purchase Manual. The bidders should participate this tender through E-Tendering System. Tender cost and EMD should be submitted only through online. For more details Contact Ph.0487 2334144.

sd/-  
**Principal**

### Approval Valid

Digitally Approved By  
Dr. Satish K P  
Date: 11.08.2023  
Reason: Approved

Forwarded / By Order  
~~Accounts Officer~~  
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