CODE	COURSE NAME	CATEGORY	L	T	P	CREDIT
EET332	COMPUTER ORGANIZATION	PEC	2	1	0	3

Prerequisite: The basic objective of this course is to lay the foundation of hardware organization of digital computers. The basic organizational concepts of Processor, Control Unit, Memory and I/O units are systematically included in this course. The knowledge on interplay between various building blocks of computer is also covered in this syllabus.

Course Outcomes: After the completion of the course, the student will be able to:

CO 1	Identify the functional units of a digital computer and understand the bus structure to do data transfer.
CO 2	Identify the pros and cons of different types of control unit design for various architectures
CO 3	Explain the principle of operation of ALU for typical arithmetic and logic operations
CO 4	Identify memory organization, Cache memory and virtual memory techniques.
CO 5	Select appropriate interfacing standards for I/O devices.

Mapping of course outcomes with program outcomes

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO 1	3	1			1							1
CO 2	3	1										1
CO 3	3	1			1							1
CO 4	2											1
CO 5	2											1

Assessment Pattern

Bloom's Category	Continuous Assessment Tests		End Semester Examination
	1	2	
Remember	10	10	20
Understand	15	15	40
Apply	25	25	40
Analyse			
Evaluate			
Create			

End Semester Examination Pattern: There will be two parts; Part A and Part B. Part A contains 10 questions (each carrying 3 marks) with 2 questions from each module. Students should answer all questions. Part B contains 2 questions from each module, out of which students should answer any one. Each question can have maximum 2 sub-divisions and carries 14 marks.

Course Level Assessment Questions

Course Outcome 1 (CO1):

1. The register R1 = 12, and R2= 13. The instruction ADD R1, R2 is in memory location 2000H. After the execution of the instruction, write the value of PC, MAR, IR and R1. Explain the instruction cycle highlighting the sub-cycles.
2. The execution time of a program on machine X is 22 nanoseconds and execution time of the same program on machine Y is 0.1 microsecond. What is the speedup of machine X over machine Y?
3. Differentiate between RISC and CISC systems.

Course Outcome 2 (CO2):

1. Consider a processor having single bus organization of the data path inside a processor. Write the sequence of control steps required for instruction: Add the contents of memory location NUM to register R1.

2. With a neat block diagram, explain in detail about micro programmed control unit and explain its operations.

Course Outcome 3 (CO3):

1. Explain the different methods for representing integers in computer systems.

2. Explain Booth's multiplication algorithm with an example.

Course Outcome 4 (CO4):

1. Show the organization of virtual memory address translation based on fixed length pages

2. Illustrate the implementation of cache memory with any two mapping functions.

Course Outcome 5 (CO5):

1. How vectored interrupts are implemented in processors?

2. Explain DMA method of data transfer in detail with suitable diagrams

Model Question paper

QP CODE:

PAGES:2

Reg.No:_____
Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY
SIXTH SEMESTER B.TECH DEGREE EXAMINATION,
MONTH & YEAR

Course Code: EET332

Course Name: Computer Organization

Max. Marks: 100 Duration: 3 Hours

PART A (3 x 10 = 30 Marks)

Answer all Questions. Each question carries 3 Marks

1. Explain Von-Neumann architecture
2. Differentiate between direct and indirect addressing modes with suitable examples
3. List the steps of a typical memory read operation.
4. Explain control word and microroutine.
5. Explain floating point representation of an integer.
6. What is the binary representation of decimal number 124.25?
7. What does memory hierarchy mean? What is its significance?
8. Explain the importance of cache memory in computer system.
9. Enlist characteristics of I/O devices
10. What are vectored interrupts?

PART B (14 x 5 = 70 Marks)
Answer any one full question from each module. Each question carries 14 Marks

Module 1

11. a). With the help of a block schematic explain the basic organizational units of a digital computer. **(7)**
    b). What is meant by addressing mode? Explain absolute and indirect addressing modes with suitable examples. **(7)**

12. a). With the help of suitable diagrams explain the single bus and multi bus organization of a computer **(8)**
    b). Differentiate between RISC and CISC systems. **(6)**

Module 2

13. a). Differentiate the design and working of hard wired and micro programmed control unit. **(8)**
    b). Write notes on instruction sequencing. **(6)**

14. a). Consider a 32-bit machine where an instruction (ADD R1, R2) is stored at location 102A (in hexadecimal). How many memory accesses are required to execute this instruction? In addition, what will be the content of PC after the instruction is fetched? Individual instruction is 16-bit. Also write the steps carried out for executing this instruction. **(8)**
    b). Illustrate the load and store cycle with an example? **(6)**

Module 3

15. a).Explain the different methods for representing integers in computer systems. **(6)**
    b). Explain Booth's multiplication algorithm with an example. **(8)**

16. a) Illustrate the methods used for representing a character **(5)**
    b). Explain non-restoring division algorithm with an example **(9)**

Module 4

17. a) Illustrate the implementation of cache memory. **(6)**
    b). Write notes on any two mapping function related to cache memory. **(8)**

18. a). How pipelining is carried out effectively in a computer system. **(8)**
    b). Differentiate various pipeline hazards **(6)**

Module 5

19. a)Explain the different types and characteristics of I/O devices. **(5)**
    b).Explain DMA method of data transfer in detail. **(9)**

20. a). Explain interrupt driven I/O techniques **(9)**
    b). Discuss the advantages and disadvantages of setting interrupt priorities **(5)**

Syllabus

Module 1

Basic Structure of Computers- functional units--Von-Neumann architecture- basic operational concepts, Introduction to buses, Measuring performance: evaluating, comparing and summarizing. Representation of Instructions: Instruction formats -Operands- Addressing modes, Instruction set architectures - CISC and RISC architectures.

Module 2

Processor and Control Unit: Fundamental Concepts, multiple bus organization of CPU, memory read and memory write operations - Data transfer using registers. Execution of a complete instruction -sequencing of control signals. Hardwired Control, Micro programmed Control

Module 3

Data representation: Signed number representation, fixed and floating point representations, character representation. Computer Arithmetic: Integer Addition and Subtraction - Booths Multiplication- Division- non- restoring and restoring techniques.

Module 4

Memory Organization: - Memory cells- Basic Organization. Memory hierarchy - Caches - Cache performance - Virtual memory - Common framework for memory hierarchies Introduction to Pipelining- Pipeline Hazards

Module 5

Input/output organisation- Characteristics of I/O devices, Data transfer schemes - Programmed controlled I/O transfer, Interrupt controlled I/O transfer. Organization of interrupts - vectored interrupts – Servicing of multiple input/output devices – Polling and daisy chaining schemes. Direct memory accessing (DMA).

Text Books

1. Hamacher C., Z. Vranesic and S. Zaky, Computer Organization, 5/e, McGraw Hill, 2011.
2. William Stallings, Computer Organization and Architecture: Designing for Performance, Pearson, 9/e, 2013.
3.

Reference Books

1. Patterson D.A. and J. L. Hennessey, Computer Organization and Design, 5/e, Morgan Kauffmann Publishers, 2013.
2. Heuring V. P. and Jordan H. F., Computer System Design and Architecture, Addison Wesely, 2/e,

Course Contents and Lecture Schedule

Sl. No.	Topic	No. of Lectures
1	**Module 1 (8 hours)**	
1.1	Basic Structure of Computers- functional units-basic operational concepts	1
1.2	Introduction to buses,Performance of computer	2
1.3	Representation of Instructions: Machine instructions-Operands-Addressing modes	2
1.4	Instruction formats, Instruction sets, Instruction set architectures	2
1.5	CISC and RISC architectures.	1
2	**Module 2(8 hours)**	
2.1	Processor and Control Unit : Some Fundamental Concepts	1
2.2	Execution of a Complete Instruction	2
2.3	Multiple Bus Organization	2
2.4	Hardwired Control, Microprogrammed Control	3
3	**Module 3(8 hours)**	
3.1	Computer arithmetic: Signed and unsigned numbers - Addition and subtraction	2
3.2	Booths algorithm,	2
3.3	Division algorithm	2
3.4	Floating point representation	2
4	**Module 4(6 hours)**	
4.1	Memory Organization: - Memory cells- Basic Organization	1
4.2	Memory hierarchy - Caches - Cache performance	2
4.3	Virtual memory	2
4.4	Introduction to pipelining-pipeline Hazards	1
5	**Module 5(6 hours)**	
5.1	Input-Output Organization: Characteristics, data transfer schemes	2
5.2	Organization of interrupts - vectored interrupts	1

5.3	Polling and daisy chaining schemes.	1
5.4	Direct memory accessing (DMA).	2