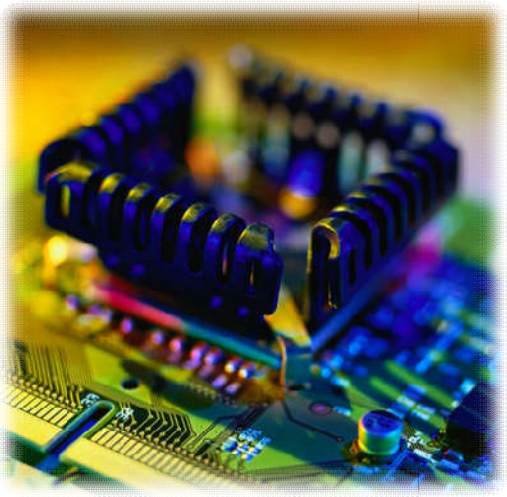
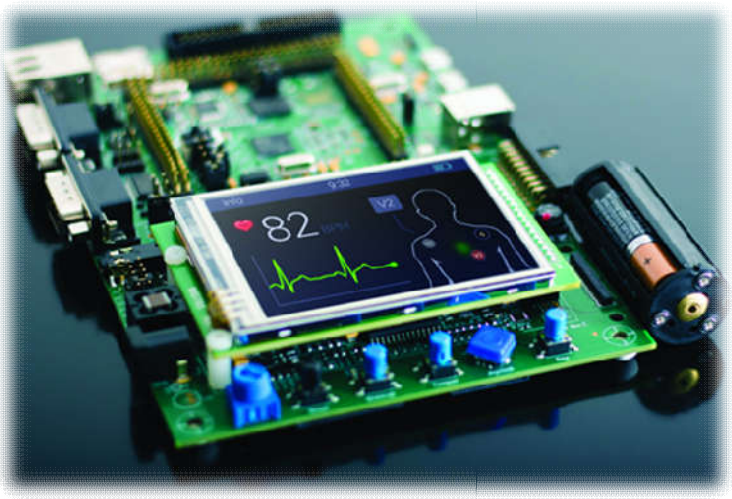
APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

(Thrissur Cluster-07)

Scheme & Syllabi

M. Tech. in





VLSI and Embedded Systems

Department of

Electronics & Communication Engineering

CLUSTER LEVEL GRADUATE PROGRAM COMMITTEE

1	Dr. Devdas Menon, Professor, IIT Madras, Chennai	Chairman
2	Principal, Government Engineering College Trichur, Thrissur	Convener
3	Principal, AXIS College of Engineering & Technology, EastKodaly, Murikkingal, Thrissur	Member
4	Principal, IES College of Engineering, Chittilappilly, Thrissur	Member
5	Principal, MET'S School of Engineering, Mala, Thrissur	Member
6	Principal, Royal College of Engineering & Technology, Akkikkavu, Thrissur	Member
7	Principal, Vidya Academy of Science & Technology, Thalakkottukara, Thrissur	Member
8	Principal, Thejus Engineering College, Vellarakkad, Erumappetty, Thrissur	Member
9	Principal, Universal Engineering College, Vallivattom, Konathakunnu, Thrissur	Member
10	Principal, Sahrdaya College of Engineering & Technology,Kodakara, Thrissur	Member

CERTIFICATE

This is to certify that

1. The scheme and syllabi are prepared in accordance with the regulation and guidelines issued by the KTU from time to time and also as per the decisions made in the CGPC meetings.
2. The suggestions/modifications suggested while presenting the scheme and syllabi before CGPC on 23.11.2020 have been incorporated.
3. There is no discrepancy among the soft copy in MS word format, PDF and hard copy of the syllabi submitted to the CGPC.
4. The document has been verified by all the constituent colleges.

Coordinator in charge of syllabus revision of the programme

(Name, designation and College Name)

Principal of the lead college

(Name and Name of the College)

Principals of the colleges in which the programme is offered

Name of the college	Principal's Name	Signature
Government Engineering College Trichur, Thrissur	Dr. V.S. Sheeba	

Date:

Place: Chairman

VLSI and Embedded Systems

Vision

To achieve academic excellence through quality education in the areas of VLSI and Embedded Systems Design.

Mission

To impart quality education by providing excellent learning and research environment, enabling the students to apply innovative techniques to address the challenges in the rapidly growing fields of VLSI design and Embedded System development for the benefit of humanity.

PROGRAM EDUCATIONAL OBJECTIVES (PEOs)

1. To meet the requirements of talented research and development professionals, solving real-life problems arising in the fields of VLSI design and Embedded System development.
2. To cater the needs of engineering professionals in the area of VLSI and Embedded Systems.
3. To foster the students' ability to think differently so that they develop into entrepreneurs, opening their own business enterprises.
4. To train the students to meet the requirements in the modern multi-disciplinary research scenario.

PROGRAM OUTCOMES (POs)

At the end of the program the student should be able to

1. Apply the knowledge gained from the Engineering courses to research problems in the area of VLSI and Embedded Systems.
2. Design/ Model VLSI and Embedded architectures for research applications, conduct performance evaluation and compare with the results reported in literature.
3. Function effectively in groups to undertake projects in interdisciplinary areas.
4. To analyze, design and implement Analog, Digital and Mixed Signal Circuits and real-time embedded systems.
5. Understand the significance of professional and ethical responsibility.
6. Communicate effectively with the technical community and disseminate the knowledge acquired to the benefit of society.
7. Understand the impacts of technical solutions to engineering problems on the society.
8. Recognize the importance and need for an active and co-operative lifelong-learning attitude.
9. Understand the prevailing professional and societal issues.
10. Develop skills to apply modern engineering tools and techniques.

M. Tech Program in VLSI and Embedded Systems - Scheme

Semester - 1

Exam Slot	Course Code	Name	L- T - P	Internal Marks	End Semester Exam		Credits
					Marks	Hrs	
A	07EC6601	VLSI Technology	4-0-0	40	60	3	4
B	07EC6603	Digital Integrated Circuit Design	4-0-0	40	60	3	4
C	07EC6605	Advanced Digital Design	4-0-0	40	60	3	4
D	07EC6607	System Design using PIC Microcontroller	3-0-0	40	60	3	3
E	07EC6XX9	Elective I	3-0-0	40	60	3	3
-	07GN6001	Research Methodology	0-2-0	100	0	0	2
-	07EC6611	Embedded Systems Lab	0-0-2	100	0	0	1
-	07EC6613	Introduction to Seminar	0-0-1	-	-	-	-
		Total	23	400	300		21

List of Electives –I

Exam Slot	Course Code	Course Name
E	07EC6609	Semiconductor Device Theory and Modeling
E	07EC6619	Semiconductor Power Devices
E	07EC6629	Python for SBC
E	07EC6639	Electric Vehicles and Architectures
E	07EC6229	Digital Image Processing
E	07EC6249	R F System Design
E	07EC6409	Electronic System Design

Semester - 2

Exam Slot	Course Code	Name	L- T - P	Internal Marks	End Semester Exam		Credits
					Marks	Hrs	
A	07EC6602	Analog Integrated Circuit Design	4-0-0	40	60	3	4
B	07EC6604	Digital Signal Processor based System Design	3-0-0	40	60	3	3
C	07EC6606	Embedded and Real-time Operating Systems	3-0-0	40	60	3	3
D	07EC6XX8	Elective II	3-0-0	40	60	3	3
E	07EC6XX2	Elective III	3-0-0	40	60	3	3
-	07EC6614	Seminar I	0-0-2	100	0	0	2
-	07EC6616	Mini Project	0-0-4	100	0	0	2
-	07EC6618	VLSI Design Lab	0-0-2	100	0	0	1
		Total	24	500	300		21

List of Electives –II

Exam Slot	Course Code	Course Name
D	07EC6628	Nano-scale Devices
D	07EC6638	Custom Digital CMOS System Design
D	07EC6648	IoT Architecture and Protocols
D	07EC6658	Automotive Embedded Systems
D	07EC6668	Embedded Product Development

List of Electives –III

Exam Slot	Course Code	Course Name
E	07EC6612	VLSI Design Automation
E	07EC6622	Testing of VLSI Circuits
E	07EC6632	Design with ARM microcontrollers
E	07EC6642	Embedded Linux Systems
E	07EC6652	Principles of Co-design
E	07EC6262	High Speed Digital Systems

Semester - 3

Exam Slot	Course Code	Name	L- T - P	Internal Marks	End Semester Exam		Credits
					Marks	Hrs	
A	07EC7XX1	Elective IV	3-0-0	40	60	3	3
B	07EC7XX3	Elective V	3-0-0	40	60	3	3
-	07EC7605	Seminar II	0-0-2	100	-	-	2
-	07EC7607	Project (Phase I)	0-0-12	50	-	-	6
		Total	20	230	120		14

List of Electives IV

Exam Slot	Course Code	Course Name
A	07EC7601	Mixed Signal Integrated Circuit Design
A	07EC7611	Emerging Architectures for Machine Learning
A	07EC7621	Embedded Applications in Power Electronics
A	07EC7631	Electronic Packaging and Reliability
A	07EC7211	Wireless Sensor Networks
A	07EC7501	VLSI Signal Processing

List of Electives V

Exam Slot	Course Code	Course Name
B	07EC7603	CMOS RF Circuit Design
B	07EC7613	Design of ASIC & SoC
B	07EC7623	Low Power VLSI
B	07EC7633	MEMS & NEMS
B	07EC7643	Embedded Network Protocols
B	07EC7653	RTOS for Multi-core Environment

Semester - 4

Exam Slot	Course Code	Name	L- T - P	Internal Marks	External Evaluation Marks	Credits
-	07EC7602	Project (Phase II)	0-0-21	70	30	12
		Total	21			12

Total: 68 Credits

SEMESTER -1
SYLLABI

Course code	Course Name	L-T-P-Credits	Year
07EC6601	**VLSI TECHNOLOGY**	**4-0-0-4**	**2020**
Pre-requisite(s)	Nil	Total Hours : 56	

COURSE OBJECTIVES

- To review the basics of MOS transistor
- To give an understanding on the wafer preparation methods
- To impart knowledge on oxidation and diffusion techniques
- To impart in-depth knowledge about different lithography methods and etching processes
- To explain the isolation techniques used in VLSI fabrication

SYLLABUS

MOS transistor, Characteristics, short channel effects, Calculation of threshold voltage of MOSFETs, Expression for drain current of MOSFETs, Body effect, Circuit model of MOSFETs including body effect, Production of metallurgical and electronic grade silicon. Crystal and wafer preparation, Lithographic techniques, Photolithography, Etching, chemical vapour deposition and ion implantation. Oxidation, Diffusion, Isolation, Metallization.

COURSE OUTCOME

On completion of the course the student will be able to

1. Explain the basics of MOS transistor.
2. Explain the purification and wafer preparation methods.
3. Describe the oxidation and diffusion techniques.
4. Explain the different lithography methods and etching process.
5. Explain the isolation techniques used in VLSI fabrication.

TEXT BOOKS

1. James D. Plummer, Michael D. Deal and Peter B. Griffin, Silicon VLSI Technology, Pearson Education, 2001
2. Adel S. Sedra and Kenneth C. Smith, Microelectronic Circuits, 5th Ed., Oxford University Press, 2004.

REFERENCES

1. Wolf S. and Tauber, R.N., Silicon Processing for the VLSI Era, Lattice Press, Sunset Beach, 2000.
2. Jaeger R.C., Introduction to Microelectronic Processing, Prentice Hall
3. Jacob Millman and Christos C. Halkias, Integrated Electronics, Tata McGraw-Hill
4. Sze S.M., Physics of Semiconductor Devices, John Wiley and Sons, 3rd Ed.
5. Ben G. Streetman and Sanjay Kumar Banerjee, Solid State Electronic devices, 6th Ed., Prentice-Hall of India, 2006.
6. Sorab K Gandhi, VLSI Fabrication Principles, John Wiley & Sons, New York, 1994
7. Nandita Das Gupta and Amitava Das Gupta, Semiconductor Devices, Prentice-Hall of India, 2004.

NPTEL/ OTHER VIDEO RESOURCES

INTERNAL ASSESSMENT: 40 MARKS

Assessment procedure:

Two internal tests, each having 15%

Tutorials/Assignments/ Mini projects having 10%

End Semester examination having 60%

Module	COURSE PLAN Contents	Contact hours	Semester Exam Marks (%)
I	Advantages of using MOSFETs as the active device in VLSI design, Structure of MOSFET and principle of operation, Ideal MOS structure, Calculation of threshold voltage for the ideal MOS structure, Modification of threshold voltage for non- ideal MOS structures, Analysis to obtain drain current as a function of gate-to-source voltage, Channel length modulation and Early voltage, Calculation of g_m and r_o, Substrate bias effect (Body effect), Transconductance due to body effect.	9	15%
II	Production of metallurgical grade silicon, Zone refining and Float zone refining methods to obtain electronic grade silicon, Czochralski technique of crystal growth, Wafer preparation, Characterization methods and wafer specifications, defects in Si and GaAs.	9	15%
	INTERNAL TEST 1		
III	Oxidation: Kinetics of oxidation, oxidation rate constants, Dopant redistribution, oxide charges Diffusion: Theory of Diffusion, Infinite Source, doping profile, Diffusion systems.	9	15%

IV	Ion Implantation Process, ion implant distributions, implantation damage and annealing. Lithographic techniques- Contact, proximity, and projection printing methods. Dependence of "feature size" on lithographic technique. Electron beam lithography.	10	15%
	INTERNAL TEST 2		
V	Etching methods- Dry and Wet Etching methods. Chemical vapour deposition techniques, Epitaxial growth, Metallization, Problems in Aluminum metal Contacts.	10	20%
VI	Isolation of components, Junction isolation and dielectric isolation. CMOS technology, Latch up in CMOS, BiCMOS technology.	9	20%
	END SEMESTER EXAMINATION		

Course code	Course Name	L-T-P-Credits	Year
07EC6603	**DIGITAL INTEGRATED CIRCUIT DESIGN**	**4-0-0-4**	**2020**
Pre-requisite(s)	Nil	Total Hours : 56	

COURSE OBJECTIVES

- To provide rigorous foundation in MOS and CMOS digital circuits

SYLLABUS

The MOS Transistor, The Wire, The CMOS Inverter, Designing Combinational Logic Gates in CMOS, Designing Sequential Logic Circuits, Interconnects, Timing Issues in Digital Circuits.

COURSE OUTCOME

On completion of the course the student will be able to

1. Understand various parameters of MOS Transistor and the Wires.
2. Analyse the static and dynamic behaviour of CMOS Inverter.
3. Design the Combinational Logic Gates in CMOS.
4. Design the Sequential Logic Circuits.
5. Understand the Interconnects.
6. Understand the Timing Issues in Digital Circuits.

TEXT BOOKS

1. Rabaey, Chandrakasan and Nikolic, "Digital Integrated Circuits – A Design Perspective", Pearson Education.

REFERENCES

1. R. Jacob Baker, Harry W. Li, David E. Boyce, "CMOS, Circuit Design, Layout, and Simulation", Wiley Interscience.
2. John P. Uyemura "Introduction to VLSI Circuits and Systems", John Wiley & Sons, Inc.
3. Sung-Mo Kang, Yusuf Leblebici, "CMOS Digital Integrated Circuits-Analysis and Design", Tata McGraw-Hill Education.
4. Neil H.E. Weste and David Money Harris, "CMOS VLSI Design-AC circuits and Systems Perspective", Pearson Education.

NPTEL/ OTHER VIDEO RESOURCES

INTERNAL ASSESSMENT: 40 MARKS

Assessment procedure:

Two internal tests, each having 15%

Tutorials/Assignments/ Mini projects having 10%

End Semester examination having 60%

Module	COURSE PLAN Contents	Contact hours	Semester Exam Marks (%)
I	The Devices: The Diode, The MOS Transistor, Process Variations, Technology Scaling. The Wire: A First Glance. Interconnect Parameters—Capacitance, Resistance, and Inductance. Electrical Wire Models. SPICE Wire Models.	9	15%
II	The CMOS Inverter: The Static CMOS Inverter, The Static Behaviour. The Dynamic Behaviour. Power, Energy, and Energy-Delay. Technology Scaling and Its Impact on the Inverter Metrics.	9	15%
	INTERNAL TEST 1		
III	Combinational Logic Gates in CMOS: Static CMOS Design, Dynamic CMOS Design, Choosing a Logic Style, Gate Design in the Ultra Deep-Submicron Era.	10	15%
IV	Sequential Logic Circuits: Timing Metrics for Sequential Circuits, Classification of Memory Elements, Static Latches and Registers, Dynamic Latches and Registers, Pulse Registers. Sense-Amplifier Based Registers, Pipelining: An Approach to Optimize Sequential Circuits, Non-Bistable Sequential Circuits, Choosing a Clocking Strategy.	10	15%
	INTERNAL TEST 2		
V	Interconnects: Capacitive Parasitics, Resistive Parasitics, Inductive Parasitics, Advanced Interconnect Techniques, Networks-on-a-Chip.	9	20%
VI	Timing Issues in Digital Circuits: Timing Classification of Digital Systems, Synchronous Design, Self-Timed Circuit Design, Synchronizers and Arbiters, Clock Synthesis and Synchronization Using a Phased-Locked Loop.	9	20%
	END SEMESTER EXAMINATION		

Course code	Course Name	L-T-P-Credits	Year
07EC6605	**ADVANCED DIGITAL DESIGN**	**4-0-0-4**	**2020**
Pre-requisite(s)	Knowledge on logic circuit design	Total Hours : **56**	

COURSE OBJECTIVES

This Course provides insights on

- Analysis and design of synchronous and asynchronous sequential circuits.
- Architectures of programmable devices.
- Fault testing procedure for combinational circuits and PLA circuits.
- Design and implementation of digital circuits using programming tools.

SYLLABUS

Sequential Circuit Design, Asynchronous Sequential Circuits, Design with State Machine Charts, Synchronous Design Using Programmable Devices, Fault Diagnosis and Testability Algorithms, System Design Using Verilog HDL.

COURSE OUTCOME

On completion of the course the student will be able to

1. Analyze and design synchronous sequential circuits.
2. Analyze hazards and design asynchronous sequential circuits.
3. Design and realize state machine charts of circuits.
4. Design PLD and ROM.
5. Understand the testing procedure for combinational circuits and PLA.
6. Design and use programming tools for implementing digital systems.

INTERNAL ASSESSMENT: 40 MARKS

Assessment procedure:

Two internal tests, each having 15%

Tutorials/Assignments/ Mini projects having 10%

End Semester examination having 60%

TEXT BOOKS

1. Charles H.Roth Jr, "Fundamentals of Logic Design" Thomson Learning 2004.
2. M.D.Ciletti,"Modeling, Synthesis and Rapid Prototyping with the Verilog HDL" Prentice Hall,1999.
3. M.G.Arnold, 'Verilog Digital – Computer Design, Prentice Hall (PTR)", 1999.
4. Nripendra N Biswas, "Logic Design Theory" Prentice Hall of India, 2001.
5. Parag K. Lala, "Fault Tolerant and Fault Testable Hardware Design", B S Publications, 2002.
6. Parag K. Lala, "Digital system Design using PLD" B S Publications, 2003.
7. S. Palnitkar, "Verilog HDL – A Guide to Digital Design and Synthesis", Pearson, 2003.

REFERENCES

1. "Digital Design Fundamentals", Kenneth J Breeding, Prentice Hall, Englewood Cliffs, New Jersey.1989.
2. "A Systematic Approach to Digital Design", William I. Fletcher, PHI, 1996.
3. "Introduction to Digital Design", James E. Palmer, David E. Perlman, Tata McGraw Hill, 1996.
4. "Logic Synthesis", S.Devadas, A.Ghosh and K.Keutzer, McGraw Hill, 1994.
5. "Logic Design Theory", N.N Biswas, Prentice Hall of India, 1st Edn,1993.
6. "Digital Design Principles and Practices", John F.Wakerly, Prentice Hall,4th Edition, 2001

NPTEL/ OTHER VIDEO RESOURCES

Module	COURSE PLAN Contents	Contact hours	Semester Exam Marks (%)
I	Sequential Circuit Design: Clocked Synchronous State Machine Analysis, Mealy and Moore machines. Finite State Machine design procedure, derive state diagrams and state tables, state reduction methods, and state assignments. Design examples using the Finite State Machine approach-sequence detector, serial adders, multipliers.	9	15%
II	Asynchronous Sequential Circuits: Analysis, Derivation of excitation table, Flow table reduction, State assignment, Transition table, Design of asynchronous Sequential circuits, Race conditions and cycles, Static and dynamic hazards, Essential hazards, Methods for avoiding races and hazards	9	15%
	INTERNAL TEST 1		
III	Design with State Machine Charts: State machine charts, Derivation of SM charts and Realization of SM charts. Implementation of Binary Multiplier, dice game controller	9	15%
IV	Synchronous Design Using Programmable Devices: Programming logic device families, Designing a synchronous sequential circuit using PLA/PAL, Designing ROM with PLA, Realization of finite state machine using PLD, FPGA, Xilinx FPGA, Xilinx 4000	9	15%
	INTERNAL TEST 2		

V	Fault Diagnosis and Testability Algorithms: Fault table method, path sensitization method, Boolean difference method, D algorithm, Kohavi algorithm, Tolerance techniques, The compact algorithm, Fault in PLA, Test generation, DFT schemes, Built in self test.	10	20%
VI	System Design Using Verilog HDL: Hardware Modeling with Verilog HDL, Logic System, Data Types and Operators for Modeling in Verilog HDL, Behavioral Descriptions in Verilog HDL, HDL Based Synthesis, Synthesis of Finite State Machines, Structural modeling, Compilation and Simulation of Verilog code, Test bench, Realization of combinational and sequential circuits using Verilog HDL.	10	20%
	END SEMESTER EXAMINATION		

Course code	Course Name	L-T-P-Credits	Year
07EC6607	**SYSTEM DESIGN USING PIC MICROCONTROLLER**	**3-0-0-3**	**2020**
Pre-requisite(s)	Basic knowledge of Digital Electronics	Total Hours : 42	

COURSE OBJECTIVES

- Upon completion of this course, the students will be able to design and implement embedded systems using PIC microcontrollers

SYLLABUS

Microcontroller: Brief history of the PIC microcontroller - PIC18 features and block diagram-PIC18 Architecture and Instruction set, Assembly language Programming, SFRs, RISC architecture in the PIC, Branch, Call, Time delay loop, PIC I/O Port programming, Addressing modes, look-up table and table processing, Bank switching in the PIC18, Data types and time delays in assembly C, I/O Port programming in C, Bit-addressable I/O programming, logic operations in C, Data conversion programs in C., PIC Peripherals and Interfacing: PIC18 timer programming in assembly and C, Serial Port programming, LCD interfacing, Matrix keyboard interfacing, ADC and DAC, PIC 18F interrupts, Programming Timer interrupts, external hardware interrupts, serial port interrupt and Port B change interrupt (Interrupt programming in assembly and C), CCP and ECCP programming, DC Motor interfacing and PWM, Stepper motor Interfacing.

COURSE OUTCOME

On completion of the course the student will be able to

1. Explain the architecture of PIC18F processor architecture
2. Understand the addressing modes and bank switching
3. Develop programs for interfacing Timer and Serial Communication modules
4. Develop programs for interfacing using LCD, Matrix keyboard, ADC and DAC
5. Develop programs using interrupts
6. Develop programs for interfacing using CCP and ECCP modules

TEXT BOOKS

1. PIC Microcontroller and Embedded Systems using assembly and C for PIC18 – Muhammad Ali Mazidi, Roind D. Mckinay, Danny Causey; Pearson Education

REFERENCES

1. Design with PIC microcontroller – John Peatman; Prentice Hall
2. Rajkamal; "Embedded Systems Architecture; Programming and Design"; Tata McGraw Hill Publications Digital Signal Processing - A Student Guide,1st Edition; T.J. Terrel and Lik-Kwan Shark; Macmillan Press Ltd.

NPTEL/ OTHER VIDEO RESOURCES

INTERNAL ASSESSMENT: 40 MARKS

Assessment procedure:

Two internal tests, each having 15%

Tutorials/Assignments/ Mini projects having 10%

End Semester examination having 60%

Module	COURSE PLAN Contents	Contact hours	Semester Exam Marks (%)
I	Microcontroller: Brief history of the PIC microcontroller - PIC18 features and block diagram- PIC18 Architecture and Instruction set, Assembly language Programming, SFRs, RISC architecture in the PIC, Branch, Call, Time delay loop, PIC I/O Port programming	7	15%
II	Addressing modes, look-up table and table processing, Bank switching in the PIC18, Data types and time delays in assembly C, I/O Port programming in C, Bit-addressable I/O programming, logic operations in C, Data conversion programs in C.	7	15%
	INTERNAL TEST 1		
III	PIC Peripherals and Interfacing: PIC18 timer programming in assembly and C, Serial Port programming in assembly & C,	7	15%
IV	LCD interfacing, Matrix keyboard interfacing, ADC and DAC interfacing (Programming in assembly & C)	7	15%
	INTERNAL TEST 2		
V	PIC 18F interrupts, Programming Timer interrupts, external hardware interrupts, serial port interrupt and Port B change interrupt (Interrupt programming in assembly and C)	7	20%
VI	CCP and ECCP programming, DC Motor interfacing and PWM, Stepper motor Interfacing	7	20%
	END SEMESTER EXAMINATION		

Course code	Course Name	L-T-P-Credits	Year
07EC6609	**SEMICONDUCTOR DEVICE THEORY AND MODELING**	**3-0-0-3**	**2020**
Pre-requisite(s)	Nil	Total Hours : 42	

COURSE OBJECTIVES

- To derive the equations, approximations and techniques available for deriving a model with specified properties
- To enable students to apply suitable approximations and techniques to derive the model referred to above.
- To offer clues to qualitative understanding of the physics of a new device
- To give understanding on how the equations get lengthy and parameters increase in number while developing a compact model
- To enable the students to describe the classification of device models

SYLLABUS

Semi-classical Bulk Transport, Drift-Diffusion Transport Model, Characteristic times and lengths associated with the bulk carrier population under equilibrium, Energy band diagrams, Steps of Deriving a Device Model, Types of Device Models, MOSFET Model.

COURSE OUTCOME

On completion of the course the student will be able to

1. Explain the equations, approximations and techniques available for deriving a model with specified properties
2. Apply suitable approximations and techniques to derive the model referred to above starting from drift-diffusion transport equations
3. Offer clues to qualitative understanding of the physics of a new device and conversion of this understanding into equations
4. Explain how the equations get lengthy and parameters increase in number while developing a compact model
5. Describe the classification of device models

TEXT BOOKS

1. M. Lundstrom,"Fundamentals of Carrier Transport", Cambridge University Press, 2000.
2. C.Snowden,"Introduction to Semiconductor Device Modeling", World Scientific, 1986.
3. Y. Tsividis and C. McAndrew,"MOSFET modeling for Circuit Simulation", Oxford University Press, 2011.

REFERENCES

1. T.A. Fjeldly, T.Ytterdal and M.Shur, "Introduction to Device Modeling and Circuit Simulation", John Wiley, 1998.
2. Y. Taur and T. H. Ning, "Fundamentals of Modern VLSI Devices", Cambridge University Press, 1998.

NPTEL/ OTHER VIDEO RESOURCES

INTERNAL ASSESSMENT: 40 MARKS

Assessment procedure:

Two internal tests, each having 15%

Tutorials/Assignments/ Mini projects having 10%

End Semester examination having 60%

Module	COURSE PLAN Contents	Contact hours	Semester Exam Marks (%)
I	Constituents of a device model. Importance of approximations in a model. Ideal and real diode modeling, Analysis, modeling, simulation and design. Levels of simulation in IC design. Semi-classical Bulk Transport – Qualitative Model	7	15%
II	Semi-classical Bulk Transport – EM field and Transport Equations.	7	15%
	INTERNAL TEST 1		
III	Drift-Diffusion Transport Model – Equations, Boundary Conditions, Mobility and Generation / Recombination.	7	15%
IV	Characteristic times and lengths, Minority carrier life time, Dielectric, momentum and energy relaxation times, Transit time and diffusion length, Debye length, Utility of characteristic times and lengths	7	15%
	INTERNAL TEST 2		
V	Energy band diagrams-E-k diagram, Utility of E-k diagram, Energy level reflecting spatial variation, Procedure for constructing an E-x diagram.	7	20%
VI	Nine Steps of Deriving a Device Model Types of device models- Classification based on voltage or current and Solution techniques.	7	20%
	END SEMESTER EXAMINATION		

Course code	Course Name	L-T-P-Credits	Year
07EC6619	**SEMICONDUCTOR POWER DEVICES**	**3-0-0-3**	**2020**
Pre-requisite(s)	Nil	Total Hours : 42	

COURSE OBJECTIVES

- To get an overview of power semiconductor switches and their structures
- To understand the static and dynamic characteristics of current controlled power semiconductor devices
- To understand the static and dynamic characteristics of voltage-controlled power semiconductor devices
- To enable the students to get the recent developments in the power semiconductor devices structures

SYLLABUS

Introduction to Power Semiconductor Devices – Power Diode - Power BJT- Power MOSFET – IGBT – Static and dynamic characteristics – Device structures – Safe Operating Area –- Base Drive and Gate Drive circuits – Recent Power semiconductor devices - SiC Devices.

COURSE OUTCOME

On completion of the course the student will be able to

1. Interpret the physics of avalanche break down mechanism in power diodes
2. Model the applications of power BJT as a switch and explore typical switching applications
3. Explain Silicon power MOSFET theory and its applications
4. Model the operation of Silicon Carbide power MOSFET theory and its applications

TEXT BOOKS

1. Power Electronics converters, applications, and design by Ned Mohan Tore M Undeland William P Robbins., John Wiley & Sons, INC.
2. Baliga, B. Jayant, Power Semiconductor Devices, PWS Publishing Co., Boston, 1996.
3. B. J. Baliga., Silicon Carbide Power Devices, World Scientific, 2006.
4. B. J. Baliga, Gallium Nitride and Silicon Carbide Power Devices, World Scientific, 2017.

REFERENCES

1. HongyuYu, TianliDuan, Gallium Nitride Power Devices, Pan Stanford 1e, 2017.
2. Erickson R. Fundamentals of Power Electronics. Kluwer Academic Publishers 2e,

NPTEL/ OTHER VIDEO RESOURCES

INTERNAL ASSESSMENT: 40 MARKS

Assessment procedure:

Two internal tests, each having 15%

Tutorials/Assignments/ Mini projects having 10%

End Semester examination having 60%

Module	COURSE PLAN Contents	Contact hours	Semester Exam Marks (%)
I	Power switching devices overview – Attributes of an ideal switch, types of power semiconductor switches– On-state and switching losses– Silicon power diodes structures - Avalanche Breakdown voltage of Silicon planar p-n junctions, Breakdown voltage Improvement Techniques, I-V characteristics, switching characteristics – rating	7	15%
II	Silicon Bipolar Power Transistor structures and characteristics, Current-gain, switching characteristics, second break down and safe operating area. Base drive circuits	7	15%
	INTERNAL TEST 1		
III	Silicon Power MOSFETs, I-V characteristics, on resistance, Minimum size chip design for specific drain breakdown voltage, Switching characteristics, Safe operating area. Gate drive circuits.	7	15%
IV	(IGBT) – Insulated Gate Bipolar Transistor Structure, Operation principle, I-V characteristics, switching characteristics, Safe operating area, Latch up and its prevention. Gate drive circuits	7	15%
	INTERNAL TEST 2		
V	Silicon Carbide power Devices – Advantages of Silicon Carbide over Silicon from high power point of view – SiC Diodes – Avalanche Breakdown Voltage - SiC Power MOSFETs	7	20%
VI	Different SiC power MOSFET architectures – on state I-V characteristics – Break down voltage improvement - SiC IGBT	7	20%
	END SEMESTER EXAMINATION		

Course code	Course Name	L-T-P-Credits	Year
07EC6629	**PYTHON FOR SBC**	**3-0-0-3**	**2020**
Pre-requisite(s)	Nil	Total Hours : 42	

COURSE OBJECTIVES

- To provide better understanding on Python basics
- To familiarize the features of Advanced Python
- To familiarize the Linux file structures and object oriented programming
- To familiarize GUI programming and Database Management
- To provide better understanding on Web programming and web server configuration
- To impart various hardware ecosystems like Raspberry Pi, BeagleBone etc.

SYLLABUS

Python Basics- Arithmetic Programs- Program Controlling- Program Loops- Advanced python- Introducing Tuples, Introducing Lists- Dictionaries and Sets- Working with Strings- Using Files-Understanding Linux File Structures- Creating Functions- Working with Modules - Understanding the Basics of Object-Oriented Programming -Employing Inheritance- Regular Expressions - Exception Handling- GUI Programming- Using the Network- Using Databases in Your Programming- Web Programming- Working with Advanced Pi/Python Projects Various hardware ecosystems: Raspberry Pi, BeagleBone, Intel Galileo, NVIDIA Jetson Nano. Comparison based on Architecture, Peripherals, Processors & on-Board Features, Board Requirements, Software and Development Tools

COURSE OUTCOME

On completion of the course the student will be able to

1. Program Python scripts
2. Create their own functions and Modules
3. Handle Linux file system using Python scripts
4. Realize the need of database and manage it accordingly
5. Develop their own GUI for specific applications
6. Configure their own web servers
7. Involve Discussions/ Practice/Exercise onto various hardware ecosystems

TEXT BOOKS

1. "Sams Teach Yourself Python Programming for Raspberry Pi in 24 Hours", Richard Blum, Christine Bresnahan Pearson Education, Inc
2. "Programming the Raspberry Pi getting started with Python" – Simin Monk McGraw Hill Edition

REFERENCES

REFERENCE NOTES/DATA SHEETS/ E-BOOKS/PPTs

NPTEL/ OTHER VIDEO RESOURCES

INTERNAL ASSESSMENT: 40 MARKS

Assessment procedure:

Two internal tests, each having 15%

Tutorials/Assignments/ Mini projects having 10%

End Semester examination having 60%

Module	COURSE PLAN Contents	Contact hours	Semester Exam Marks (%)
I	Python Basics: Formatting Scripts for Readability -Python Variables - Data Types - Python Script Output- Python Script Input. Arithmetic Programs:- Math Operators- Calculating with Fractions- Complex Number Math - math Module - NumPy Math Libraries Program Controlling:- if Statement- else Statement - elif Statement-Comparing Values in Python- Checking Complex Conditions -Negating a Condition Check Program Loops:- Repetitive Tasks -for Loop, while Loop, Nested Loops	7	15%
II	Tuples, Lists Multi-dimensional Lists-List Comprehensions- Python Dictionary Terms- Programming with Dictionaries - Python Sets - Modifying a Set, Programming with Sets Working with Strings-The Basics of Using Strings-Using Functions to Manipulate Strings-Formatting Strings for Output	6	15%
	INTERNAL TEST 1		
III	Linux File Structures- Managing Files and Directories – Opening, Reading, Closing and Writing to a File Creating Functions -Handling Variables in Function- Lists with Functions- Recursion with Functions Working with Modules- Standard Modules-Creating Custom Modules Understanding the Basics of Object-Oriented Programming-Defining Class Methods-Sharing Code with Class Modules	7	15%

IV	Inheritance-Class Problem- Subclasses and Inheritance Regular Expressions- Working with Regular Expressions - match() function - search() function - findall() and finditer() functions Exception Handling- Handling Multiple Exceptions GUI Programming- Programming for a GUI Environment- Examining Python GUI Packages-Using the tkinter Package -Exploring the tkinter Widgets	7	15%
	INTERNAL TEST 2		
V	Python Network Modules-Working with Email Servers-Working with Web Servers-Linking Programs Using Socket Programming Using Databases in Your Programming- Working with the MySQL Database -Using the PostgreSQL Database Web Programming- Running a Web Server on the Pi-Programming with the Common Gateway Interface Expanding Your Python Web pages- Processing Forms Working with Advanced Pi/Python Projects - Exploring the GPIO Interface- Using the RPi.GPIO Module Controlling GPIO Output Detecting GPIO Input	8	20%
VI	Various hardware Ecosystems,: Raspberry Pi, BeagleBone, Intel Galileo, NVIDIA Jetson Nano. Comparison based on Architecture, Peripherals, Processors & on-Board Features, Board Requirements, Software and Development Tools Introduction to Raspberry Pi SBC, history, Models, SoC specifications, Memory, Peripherals, Noobs loading, Linux Distros for Pi. Exploring the Raspberry Pi GPIO Interface- Using the RPi.GPIO Module-Controlling GPIO Output Detecting GPIO Input Blinking LED and Input polling codes using RPi.GPIO module	7	20%
	END SEMESTER EXAMINATION		

Course code	Course Name	L-T-P-Credits	Year
07EC6639	**ELECTRIC VEHICLES AND ARCHITECTURES**	**3-0-0-3**	**2020**
Pre-requisite(s)	**Nil**	Total Hours : 42	

COURSE OBJECTIVES

- To impart a fundamental knowledge of Electric Vehicles and Hybrid Vehicles

SYLLABUS

Vehicle Fundamentals – Electric Vehicles Configurations – Hybrid Electric Vehicle – Concept and Architecture – Electric Propulsion Systems – Series/ Parallel Hybrid Drive Train Designs – Energy Storage mechanism – Regenerative Braking – Planetary Gear and Double Rotor Electric Variable Transmission Systems

COURSE OUTCOME

On completion of the course the student will be able to

1. Explain the configurations of Electric Vehicles
2. Interpret the different propulsion systems applicable to Electric Vehicles
3. Compare and explain the different propulsion systems
4. Classify different Hybrid configurations of electric vehicles
5. Explain and interpret the different energy storage mechanisms in Electric Vehicles
6. Summarize the primary electric transmission system used in Electric Vehicles

TEXT BOOKS

1. Mehrdad Ehsani, Yimin Gao, "Modern Electric, Hybrid Electric, and Fuel Cell Vehicles: Fundamentals, Theory, and Design", Second Edition (Power Electronics and Applications Series) Standardsmedia (1 January 2009)
2. K. T. Chau, "Electric Vehicle Machines and Drives Design, Analysis and Application", John Wiley and Sons, 2015.
3. Iqbal Husain, "Electric and Hybrid Vehicles: Design Fundamentals", CRC Press, 2005

REFERENCES

1. James Larminie, John Lowry, "Electric Vehicle Technology Explained", John Wiley and Sons, 2003.
2. C.C. Chan and K.T. Chau, "Modern Electric Vehicle Technology", Oxford University Press, 2001

NPTEL/ OTHER VIDEO RESOURCES

INTERNAL ASSESSMENT: 40 MARKS

Assessment procedure:

Two internal tests, each having 15%

Tutorials/Assignments/ Mini projects having 10%

End Semester examination having 60%

Module	COURSE PLAN Contents	Contact hours	Semester Exam Marks (%)
I	Vehicle Fundamentals : Vehicle Resistance - Tire-Ground Adhesion and Maximum Tractive Effort – Power Train Tractive Effort and Speed - Vehicle power plant and transmission - Braking Performance Electric Vehicles – Configurations – Performance of EV – Tractive Effort in Normal Driving – Energy Consumption Hybrid Electric Vehicles – Concept - Architecture	7	15%
II	Electric Propulsion Systems – DC Motor Drives – Principle and Performance –Control mechanisms – DC motor Drives - Induction Motor Drives – Operation Principle – Power Electronic Control – Field Orientation Control – Voltage source Inverter for FOC	7	15%
	INTERNAL TEST 1		
III	Permanent Magnet Brushless DC Motor Drives – Principle of BLDC – Construction and Classification – PM Materials – Performance Analysis – Sensor-less Techniques Switched Reluctance Motor Drives – Modes of Operation – Sensor-less Control – Self tuning techniques of SRM Drives – Vibration and acoustic Noise in SRM	7	15%

IV	Series Hybrid Electric Drive Train Design – Control Strategies – Sizing of the major components – Sample design of traction motor size and Gear Ratio Parallel Hybrid Electric Drive Train Design – Control Strategies – Design of drive train parameters – Design of Engine Power Capacity – Electric Motor Drive Power Capacity Mild Hybrid Electric Drive Train Design – Parallel Mild Electric Drive Train – Operating Modes and Control strategy -Series-Parallel Mild Hybrid electric drive train – Operating modes and Control	7	15%
	INTERNAL TEST 2		
V	Energy Storages – Electrochemical Batteries – Ultra Capacitors – Ultra High Speed Flywheels – Hybridization of Energy storages. Fundamentals of Regenerative Braking	7	20%
VI	Planetary-Geared Electric Variable Transmission Systems – Planetary Gears – Input Split PG EVT Systems – Compound split PG-EVT systems Double Rotor Electric Variable transmission System – Double Rotor Machines – Basic & Advance Double Rotor EVT systems	7	20%
	END SEMESTER EXAMINATION		

Course code	Course Name	L-T-P-Credits	Year
07EC6229	**DIGITAL IMAGE PROCESSING**	**3-0-0-3**	**2020**
Pre-requisite(s)	Basic course in Digital Signal Processing	Total Hours : 42	

COURSE OBJECTIVES

- Get a thorough understanding of digital image representation and processing techniques
- Understand the various steps in digital image processing.

SYLLABUS

Image representation, Two dimensional orthogonal transforms - DFT, FFT, WHT, Haar transform, KLT, DCT, Image enhancement, histogram-based processing, homomorphic filtering, Edge detection, LOG filters, localization problem, Image Restoration using inverse filtering, Wiener filtering and maximum entropy-based methods, Mathematical morphology, gray scale morphology, applications, Image and Video Compression Standards, Sub-band Decomposition, Entropy Encoding, JPEG, JPEG2000, MPEG, Image texture analysis, statistical models for textures, Hough Transform, Computer tomography, Radon transform, Back-projection operator, Fourier slice theorem, CBP and FBP methods, ART, Fan beam projection.

COURSE OUTCOME

On completion of the course the student will be able to

1. Understand various techniques for image representation
2. Process the image in spatial and transform domain for better enhancement.

TEXT BOOKS

1. Gonzalez and Woods, Digital image processing, Prentice Hall, 2002..

REFERENCES

1. A.K. Jain, Fundamentals of digital image processing, Prentice Hall of India,1989.
2. M. Haralick, and L.G. Shapiro, Computer and Robot Vision, Vol-1, Addison Wesley, Reading, MA, 1992

NPTEL/ OTHER VIDEO RESOURCES

INTERNAL ASSESSMENT: 40 MARKS

Assessment procedure:

Two internal tests, each having 15%

Tutorials/Assignments/ Mini projects having 10%

End Semester examination having 60%

Module	COURSE PLAN Contents	Contact hours	Semester Exam Marks (%)
I	Image representation - Gray scale and colour, Images, image sampling and quantization, Two dimensional orthogonal transforms - DFT, FFT, WHT, Haar transform, KLT, DCT.	7	15%
II	Image enhancement - filters in spatial and frequency domains, histogram-based processing, homomorphic filtering	7	15%
	INTERNAL TEST 1		
III	Edge detection - non parametric and model, based approaches, LOG filters, localization problem, Image Restoration - PSF, circulant and block - circulant matrices, deconvolution, restoration using inverse filtering, Wiener, filtering and maximum entropy-based methods	7	15%
IV	Mathematical morphology - binary morphology, dilation, erosion, opening and closing, duality relations, gray scale morphology, applications such as hit-and-miss Transform, thinning and shape decomposition, Image and Video Compression Standards- Lossy and lossless compression schemes: Sub-band Decomposition, Entropy Encoding, JPEG, JPEG2000, MPEG.	7	15%
	INTERNAL TEST 2		
V	Image texture analysis: co-occurrence matrix, measures of textures, statistical models for textures. Hough Transform, boundary detection, chain coding, segmentation and thresholding methods.	7	20%
VI	Computer tomography: parallel beam projection, Radon transform, and its inverse, Back-projection operator, Fourier-slice theorem, CBP and FBP methods, ART, Fan beam projection	7	20%

Course code	Course Name	L-T-P-Credits	Year
07EC6249	**R F SYSTEM DESIGN**	**3-0-0-3**	**2020**
Pre-requisite(s)	A basic course in Electromagnetic field theory	Total Hours : 42	

COURSE OBJECTIVES

- Familiarize how to use Smith chart.
- Get an overview about the details of microwave switches and phase shifters.
- Get an idea about microwave filters.

SYLLABUS

Review of Transmission Line Theory, Lumped Element Model, SWR and Impedance Mismatches, Planar Transmission Lines Strip-line, Micro-strip, Coplanar-Line, Smith Chart, Reflection Coefficient, Load Impedance, Impedance & Admittance Transformations, Parallel and Series Connection, Revision of S-Parameters, RF Filter Design, Special Filter Realizations-Filter Implementations, Networks Impedance Matching using Discrete Components, Single& Double Stub Matching Network, Quarter-Wave Transformers, RF Amplifiers Oscillators, Mixers and their Characteristics, Stability Considerations, Constant VSWR Circles, Low Noise Circuits; Broadband High Power and Multistage Amplifiers.

COURSE OUTCOME

On completion of the course the student will be able to

1. Understand the importance of Smith chart in various design applications.
2. design microwave filters.

TEXT BOOKS

1. Reinhold Ludwig & Powel Bretchko, RF Circuit Design – Theory and Applications, IEd, Pearson Education Ltd., 2004.
2. David M. Pozzar, Microwave Engineering, 3rd, Wiley India, 2007.

REFERENCES

1. Mathew M. Radmanesh, Advanced RF & Microwave Circuit Design- The Ultimate Guide to System Design, Pearson Education Asia, 2009
2. Davis W. Alan, Radio Frequency Circuit Design, Wiley India, 2009.
3. Cotter W. Sayre, Complete Wireless Design, 2nd, McGraw-Hill, 2008.

NPTEL/ OTHER VIDEO RESOURCES

INTERNAL ASSESSMENT: 40 MARKS

Assessment procedure:

Two internal tests, each having 15%

Tutorials/Assignments/ Mini projects having 10%

End Semester examination having 60%

Module	COURSE PLAN Contents	Contact hours	Semester Exam Marks (%)
I	Transmission Line Theory: Review of Transmission Line Theory- Lumped Element Model- Field Analysis of Transmission Lines- Terminated Lossless Lines- SWR and Impedance Mismatches	7	15%
II	Planar Transmission-Lines: Strip-line, Microstrip, Coplanar-Line. Smith Chart: Reflection Coefficient- Load Impedance- Impedance Transformation- Admittance Transformation- Parallel and Series Connection- Revision of S-Parameters.	7	15%
	INTERNAL TEST 1		
III	RF Filter Design Overview; Basic Resonator and Filter Configuration- Special Filter Realizations- Filter Implementations- Coupled Filter.	7	15%
IV	Impedance Matching: Networks Impedance Matching using Discrete Components- Micro-strip line Matching Networks- Single Stub Matching Network- Double Stub Matching Network.	7	15%
	INTERNAL TEST 2		
V	Quarter-Wave Transformers- Multi-Section and Tapered Transformers, RF Amplifiers Oscillators, Mixers and their Characteristics: Amplifier Power Relations- Stability Considerations- Constant Gain Circles- Noise Figure Circles- Constant VSWR Circles	7	20%
VI	Low Noise Circuits; Broadband High Power and Multistage Amplifiers- Basic Oscillator Model- High Frequency Oscillator Configurations- Basic Characteristics of Mixers		20%
	END SEMESTER EXAMINATION		

Course code	Course Name	L-T-P-Credits	Year
07EC6409	**ELECTRONIC SYSTEM DESIGN**	**3-0-0-3**	**2020**
Pre-requisite(s)	Electronics circuits	Total Hours : 42	

COURSE OBJECTIVES

- Students will understand the Practical Analog & Mixed Signal Circuit Design Issues and Techniques as well as Practical logic Circuit Design Issues and Techniques.

SYLLABUS

Practical Analog & Mixed Signal Circuit Design Issues and Techniques, Passive components, Opamps, ADCs and DACs, power supplies, CMOS& BiCMOS family Logic devices, Design for testability, Estimating digital system reliability, Cabling of Electronic Systems, Grounding of Electronic Systems, Balancing & Filtering in Electronic Systems, Protection Against Electrostatic Discharges (ESD), Cooling in/of Electronic System: Heat transfer, approach to thermal management Packaging & Enclosures of Electronic System.

COURSE OUTCOME

On completion of the course the student will be able to

1. Design both analog and digital circuits with the knowledge of issues and Techniques.

TEXT BOOKS

1. Electronic Instrument Design, 1st edition; by: Kim R. Fowler; Oxford University Press.
2. Noise Reduction Techniques in Electronic Systems, 2nd edition; by: Henry W. Ott; John Wiley & Sons.
3. Digital Design Principles & Practices, 3rd edition by: John F. Wakerly; Prentice Hall International, Inc.
4. Operational Amplifiers and linear integrated circuits, 3rd edition by: Robert F. Coughlin; Prentice Hall International, Inc
5. Intuitive Analog circuit design by: Mark. T Thompson; Published by Elsevier

REFERENCES

1. Printed Circuit Boards - Design & Technology, 1st edition; by: W Bosshart; Tata McGraw Hill.
2. A Designer's Guide to Instrumentation Amplifiers; by: Charles Kitchin and Lew Counts; Seminar Materials @ http://www.analog.com.
3. Errors and Error Budget Analysis in Instrumentation Amplifier Applications; by: Eamon Nash; Application note AN-539 @ http://www.analog.com
4. Practical Analog Design Techniques; by: Adolofo Garcia and Wes Freeman; Seminar Materials @ http://www.analog.com
5. Selecting An A/D Converter; by:Larry Gaddy; Application bulletin @http://www.Ti.com
6. Benefits and issues on migration of 5-volt and 3.3 volt logic to lower voltage supplies; Application note SDAA011A @ http://www.Ti.com
7. JTAG/IEEE 1149.1 deigns considerations; Application note SCTA029@http://www.Ti.com
8. Live Insertion; Application note SDYA012@ http://www.Ti.com
9. PCB Design Guidelines For Reduced EMI; Application note SZZA009@http://www.Ti.com

NPTEL/ OTHER VIDEO RESOURCES

Module	COURSE PLAN Contents	Contact hours	Semester Exam Marks (%)
I	Practical Analog & Mixed Signal Circuit Design Issues and Techniques: Passive components: Understanding and interpreting data sheets and specifications of various passive and active components, non-ideal behavior of passive components,. Op amps: DC performance of op amps: Bias, offset and drift. AC Performance of operational amplifiers: band width, slew rate and noise. Properties of a high quality instrumentation amplifier. Design issues affecting dc accuracy & error budget analysis in instrumentation amplifier applications	7	15%
II	ADCs and DACs: Characteristics, interfacing to microcontrollers. Selecting an ADC, Power supplies: Characteristics, design of full wave bridge regulated power supply, Circuit layout and grounding in mixed signal system. Practical Logic Circuit Design Issues and Techniques: Understanding and interpreting data sheets & specifications of various CMOS& BiCMOS family Logic devices. Electrical behavior (steady state & dynamic) of CMOS& BiCMOS family logic devices. Benefits and issues on migration of 5-volt and 3.3 volt logic to lower voltage supplies.	7	15%
	INTERNAL TEST 1		
III	Design for testability, Estimating digital system reliability. Digital circuit layout and grounding. PCB design guidelines for reduced EMI. Electromagnetic Compatibility (EMC): Designing for (EMC), EMC regulations, typical noise path, methods of noise coupling, methods of reducing interference in electronic systems	7	15%

IV	Cabling of Electronic Systems: Capacitive coupling, effect of shield on capacitive coupling, inductive coupling, effect of shield on inductive coupling, effect of shield on magnetic coupling, magnetic coupling between shield and inner conductor, shielding to prevent magnetic radiation, shielding a receptor against magnetic fields, coaxial cable versus shielded twisted pair, ribbon cables. Grounding of Electronic Systems: Safety grounds, signal grounds, single point ground systems, multipoint-point ground systems, hybrid grounds, functional ground layout, practical low frequency grounding, hardware grounds, grounding of cable shields, ground loops, shield grounding at high frequencies	7	15%
	INTERNAL TEST 2		
V	Balancing & Filtering in Electronic Systems: Balancing, power line filtering, power supply decoupling, decoupling filters, high frequency filtering, system bandwidth. Protection Against Electrostatic Discharges (ESD): Static generation, human body model, static discharge, ESD protection in equipment design, software and ESD protection, ESD versus EMC.	7	20%
VI	Packaging & Enclosures of Electronic System: Effect of environmental factors on electronic system (environmental specifications), nature of environment and safety measures. Packaging influence and its factors. Cooling in/of Electronic System: Heat transfer, approach to thermal management, mechanisms for cooling, operating range, basic thermal calculations, cooling choices, heat sink selection	7	20%
	END SEMESTER EXAMINATION		

Course code	Course Name	L-T-P-Credits	Year
07GN6001	**RESEARCH METHODOLOGY**	**0-2-0-2**	**2020**
Pre-requisite(s)	Nil	Total Hours : 28	

COURSE OBJECTIVES

- Provide a familiarization with research methodology and to induct the student into the overall research process and methodologies.
- The scientific research process and the various steps involved
- Formulation of research problem and research design
- Thesis preparation and presentation.
- Research proposals, publications and ethics
- Important research methods in engineering

As a tutorial type course, this course is expected to be more learner centric and active involvement from the learners are expected which encourages self study and group discussions. The faculty mainly performs a facilitator's role.

SYLLABUS

Overview of research methodology - Research process, scientific method, research design process. Research Problem and Design - Formulation of research task, literature review, and web as a source, problem solving approaches, experimental research, and ex post facto research. Thesis writing, reporting and presentation -Interpretation and report writing, principles of thesis writing- format of reporting, oral presentation. Research proposals, publications and ethics - Research proposals, research paper writing, considerations in publishing, citation, plagiarism and intellectual property rights. Research methods – Modeling and Simulation, mathematical modeling, graphs, heuristic optimization, simulation modeling, measurement design, validity, reliability, scaling, sample design, data collection methods and data analysis.

COURSE OUTCOME

On completion of the course the student will be able to

1. Discuss research methodology concepts, research problems, research designs, thesis preparations, publications and research methods.
2. Analyze and evaluate research works and to formulate a research problem to pursue research
3. Prepare a thesis or a technical paper, and present or publish them
4. Apply the various research methods followed in engineering research for formulation and design of own research problems and to utilize them in their research project.

TEXT BOOK

1. C. R. Kothari, Research Methodology, Methods and Techniques, New Age International Publishers
2. K. N. Krishnaswamy, AppaIyer Sivakumar, M. Mathirajan, Management Research Methodology, Integration of principles, Methods and Techniques, Pearson Education
3. R. Panneerselvam, Research Methodology, PHILearning
4. Deepak Chawla, Meena Sondhi, Research Methodology–concepts & cases, Vikas Publg House
5. J.W Bames, Statistical Analysis for Engineers and Scientists, McGraw Hill, N.York
6. SchankFr.,TheoriesofEngineeringExperiments,TataMcGrawHillPublication.
7. WillktnsionK.L,BhandarkarP.L,FormulationofHypothesis,HimalayaPublication.
8. Fred M Kerlinger, Research Methodology
9. Ranjit Kumar, Research Methodology – A step by step guide for beginners, Pearson Education
10. John W Best, James V Kahan – Research in Education, PHILearning

REFERENCES

1. Donald R. Cooper, Pamela S. Schindler, Business Research Methods, 8/e, Tata McGraw- Hill CoLtd
2. Sinha, S.C. and Dhiman, A.K., 2002. Research Methodology, EssEss Publications. 2 volumes
3. Trochim, W.M.K., 2005. Research Methods: the concise knowledge base, Atomic Dog Publishing.270p.
4. Coley, S.M. and Scheinberg, C. A., 1990, "Proposal Writing", SagePublications.
5. Day, R.A., 1992.How to Write and Publish a Scientific Paper, Cambridge University Press.
6. Fink, A., 2009. Conducting Research Literature Reviews: From the Internet to Paper. Sage Publications
7. Donald H.McBurney, Research Methods, 5th Edition, Thomson Learning,
8. Garg, B.L., Karadia, R., Agarwal, F. and Agarwal, U.K., 2002. An introduction to Research Methodology, RBSA Publishers..
9. Wadehra, B.L. 2000. Law relating to patents, trademarks, copyright designs and geographical indications. Universal Law Publishing
10. Carlos, C.M., 2000. Intellectual property rights, the WTO and developing countries: the TRIPS agreement and policy options. Zed Books, NewYork.
11. Additional suitable web resources or Guidelines related to conference and journal publications

INTERNAL ASSESSMENT: 100 MARKS

Internal continuous assessment is in the form of periodical tests and assignments. There are three tests for the course (3 x 20 = 60 marks) and assignments (40 marks). The assignments can be in the form of seminar, group tasks, case studies, research work or in a suitable format as decided by the teacher.

Module	COURSE PLAN Contents	Contact hours	Semester Exam Marks (%)
I	Overview of Research Methodology: Research concepts – meaning – objectives – motivation - types of research – research process – criteria for good research – problems encountered by Indian researchers - scientific method - research design process- decisional research	5	10%
II	Research Problem and Design: Formulation of research task – literature review – methods – primary and secondary sources – web as a source – browsing tools -formulation of research problems – exploration - hypothesis generation - problem solving approaches-introduction to TRIZ(TIPS)- experimental research – principles -Laboratory experiment – experimental designs - ex post facto research - qualitative research	5	15%
	INTERNAL TEST 1		
III	Thesis writing, reporting and presentation Interpretation and report writing – techniques of interpretation – precautions in interpretation – significance of report writing – principles of thesis writing- format of reporting - different steps in report writing – layout and mechanics of research report - references – tables – figures – conclusions. oral presentation – preparation-making presentation–use of visual aids-effective communication	4	15%
IV	Research proposals, publications, ethics and IPR Research proposals - development and evaluation – research paper writing – layout of a research paper - journals in engineering – considerations in publishing – scientometry- impact factor- other indexing like h-index – citations - open access publication -ethical issues - plagiarism –software for plagiarism checking- intellectual property right- patenting case studies	5	15%

	INTERNAL TEST 2		
V	Research methods – Modeling and Simulation Modeling and Simulation – concepts of modeling – mathematical modeling - composite modeling – modeling with – ordinary differential equations – partial differential equations – graphs heuristics and heuristic optimization-simulation modeling	5	20%
VI	Research Methods - Measurement, sampling and Data acquisition: Measurement design - errors -validity and reliability in measurement- scaling and scale construction-sample design - sample size determination - sampling errors - data collection procedures - sources of data - data collection methods -datum preparation and data analysis	4	20%
	INTERNAL TEST 3		

Course code	Course Name	L-T-P-Credits	Year
07EC6611	**EMBEDDED SYSTEMS LAB**	**0-0-2-1**	**2020**
Pre-requisite(s)	Nil	Total Hours : 28	

COURSE OBJECTIVES

- Design enlisted experiments and implement using hardware
- Acquire sufficient expertise in simulating systems
- Synthesize Verilog design
- Familiarize PIC based Embedded System Development

TOOLS

Xilinx, Vivado & MPLAB IDE or Equivalent.

COURSE OUTCOME

On completion of the course the student will be able to

1. Design and implement self-standing systems of their choice with sufficient complexity.

INTERNAL ASSESSMENT:100 MARKS

Assessment procedure:

i) Practical Records /outputs - 40%

ii) Regular Class Viva-Voce - 20%

iii) Final Test - 40%

LIST OF EXPERIMENTS

PART A

I. FPGA Based experiments (Simulation and Synthesis)

1. MUX
2. DEMUX
3. Decoder
4. Encoder
5. Half adder and full adder
6. 4-bit ripple carry adder
7. 4-bit carry look ahead adder
8. FFs- JK,SR,D,T etc
9. Binary, Ring and Johnson's counter

PART B

II. PIC Experiments

1. Toggling of one bit of any PORT continuously
2. Reading 8 bit data as two 4 bits through any PORT
3. Sorting- Ascending/ Descending
4. Toggling a bit of a port continuously at a particular frequency and generating a count in another port
5. Program to read the status of a switch connected to a port pin
6. Get the value of x from a port and calculate x^2+3x+6 from lookup table
7. Configuring Timer 1 as an event counter
8. Generation of two square waves of different duty cycle
9. Generating PWM to control DC motor speed
10. Capturing an event
11. LCD interfacing
12. Displaying Hex values in 7 segment LED
13. External Hardware interrupt
14. Interfacing Matrix keyboard using PORT B change interrupt

Course code	Course Name	L-T-P-Credits	Year
07EC6613	**INTRODUCTION TO SEMINAR**	**0-0-1-0**	**2020**
Pre-requisite(s)	Nil	Total Hours : --	

COURSE OBJECTIVES

- To improve the debating capability of the student to present a technical topic
- To impart training to the student to face audience and present his ideas and thus creating self-esteem and courage essential for an engineer

OUTLINE

Individual students are required to choose a topic of their interest and give a seminar on that topic for about 30 minutes. A committee consisting of at least three faculty members shall assess the presentation of the seminar. The committee will provide feedback to the students about the scope for improvements in communication, presentation skills and body language. Each student shall submit one copy of the report of the seminar topic.

COURSE OUTCOME

1. The graduate will have improved the debating capability and presentation skills in any topic of his choice

SEMESTER -2
SYLLABI

Course code	Course Name	L-T-P-Credits	Year
07EC6602	**ANALOG INTEGRATED CIRCUIT DESIGN**	**4-0-0-4**	**2020**
Pre-requisite(s)	Nil	Total Hours :56	

COURSE OBJECTIVES

- To develop the ability to design and analyze MOS based Analog VLSI circuits.
- To draw the equivalent circuits of MOS based Analog VLSI and analyze their performance.
- To develop the skills to design analog VLSI circuits for a given specification.

SYLLABUS

Basic MOS Device Physics, Single-Stage Amplifiers, Differential Amplifiers, Current Mirrors and Biasing Techniques, Frequency Response of Amplifiers, Noise, Feedback, Operational Amplifiers, Stability and Frequency Compensation, Band-gap References, Introduction to Switched-Capacitor Circuits.

COURSE OUTCOME

On completion of the course the student will be able to

1. Explain the small signal models and approximations for analog circuit analysis and design.
2. Illustrate the suitable biasing for a given circuit.
3. Model single stage amplifiers for given specifications.
4. Interpret differential amplifiers and formulate design procedures of one and two stage operational amplifiers.
5. Summarize the Band-gap References and Switched-Capacitor Circuits.
6. Outline the role of feedback on oscillation and different oscillator configurations.

TEXT BOOKS

1. Behzad Razavi, "Design of Analog CMOS Integrated Circuits", Tata McGraw Hill

REFERENCES

1. R.J. Baker, H.W. Li, D.E. Boyce, CMOS Circuit design, Layout, and Simulation.
2. Gray, Hurst, Lewis, Meyer, "Analysis and Design of Analog Integrated Circuits", 5th Edition, Wiely India
3. Philip E Allen, Douglas R Holberg, "CMOS Analog Circuit Design", OUP India.
4. T.C Carusone, David A. Johns, Kenneth W.Martin, "Analog Integrated Circuit Design", Wiley.

NPTEL/ OTHER VIDEO RESOURCES

INTERNAL ASSESSMENT: 40 MARKS

Assessment procedure:

Two internal tests, each having 15%

Tutorials/Assignments/ Mini projects having 10%

End Semester examination having 60%

Module	COURSE PLAN Contents	Contact hours	Semester Exam Marks (%)
I	**Introduction to Analog Design:** Basic MOS Device Physics: General Considerations, MOS I/V Characteristics, Second-Order Effects, MOS Device Models, Behavior of a MOS Device as a Capacitor **Single-Stage Amplifiers:** Common-Source Stage, Source Follower, Common-Gate Stage, Cascode Stage, Choice of Device Models	9	15%
II	**Differential Amplifiers:** Basic Differential Pair, Common-Mode Response, Differential Pair with MOS Loads, Gilbert Cell. **Current Mirrors and Biasing Techniques:** Basic Current Mirrors, Cascode Current Mirrors, Active Current Mirrors, Biasing Techniques.	9	15%
	INTERNAL TEST 1		
III	**Frequency Response of Amplifiers:** General Considerations, Common-Source Stage, Source Followers, Common-Gate Stage, Cascode Stage, Differential Pair, Gain-Bandwidth Trade-Offs. **Noise:** review of basics **Feedback:** Review of basics, Feedback Topologies, Effect of Feedback on Noise, Effect of Loading, Bode's Analysis of Feedback Circuits, Middle-brook's Method, Loop Gain Calculation Issues, Alternative Interpretations of Bode's Method.	9	15%

IV	**Operational Amplifiers:** One-Stage Op Amps, Two-Stage Op Amps, Gain Boosting, Output Swing Calculations, Common-Mode Feedback, Input Range Limitations, Slew Rate, High-Slew-Rate Op Amps, Power Supply Rejection, Noise in Op Amps. **Stability and Frequency Compensation:** Multi-pole Systems, Phase Margin, Basic Frequency Compensation, Compensation of Two-Stage Op Amps, Slewing in Two-Stage Op Amps, Other Compensation Techniques, Nyquist's Stability Criterion	9	15%
	INTERNAL TEST 2		
V	**Bandgap References:** Supply-Independent Biasing, Temperature-Independent References, PTAT Current Generation, Constant-*Gm* Biasing, Speed and Noise Issues, Low-Voltage Bandgap References Introduction to Switched-Capacitor Circuits: Sampling Switches, Switched-Capacitor Amplifiers, Switched-Capacitor Integrator, Switched-Capacitor Common-Mode Feedback.	10	20%
VI	**Nonlinearity and Mismatch:** Nonlinearity, Mismatch Oscillators: Ring Oscillators, LC Oscillators, Voltage-Controlled Oscillators, Mathematical Model of VCOs	10	20%
	END SEMESTER EXAMINATION		

Course code	Course Name	L-T-P-Credits	Year
07EC6604	**DIGITAL SIGNAL PROCESSOR BASED SYSTEM DESIGN**	**3-0-0-3**	**2020**
Pre-requisite(s)	Basic course in Digital Signal Processing & Microprocessors and Microcontrollers (UG level).	Total Hours :42	

COURSE OBJECTIVES

- Upon completion of this course, the student will be able to design systems using the popular Digital Signal Processor Family TMS 320 C64XX/67XX.

SYLLABUS

Introduction to a popular DSP from Texas Instruments, CPU Architecture, Functional Units, CPU Data Paths and Control, Internal Data/ Program Memory, External Memory Interface, Timers, Interrupts, Pipelining, EDMA, Multi Channel Buffered Serial Port, Linear and Circular addressing Programming: Instruction Set and Addressing Modes, TMS 320C64X CPU Simple programming examples using C and assembly, Typical DSP development system, support tools and files, compiler, assembler, Code composer studio, CODECs DSP Applications: Typical CODEC architecture, Sine wave generation from table data, DTMF Tone Generation and Detection Techniques and Implementation, Voice detection and reverse playback, Filter Design: FIR & IIR Digital Filter Design programs using MATLAB Fourier Transform: DFT, FFT programs using MATLAB Implementation of Real-time Digital filters using DSP: Implementation of FFT applications using DSP, RTDX between MATLAB and CC Studio, Features of DSP controllers, peripherals (TMS 320 28XX series), Typical Architecture of DM 64XX series Da Vinci SoC processor, Current Trends in Digital Signal Processors

COURSE OUTCOME

On completion of the course the student will be able to

1. Explain the architecture of a typical DSP processor architecture
2. Develop programs in DSP platform for different applications
3. Understand the features of DSP controller, Da Vinci processor

TEXT BOOKS

1. Digital Signal Processing and Application with TMS 320 C6713 and TMS320C6416 DSK, Rulph Chassaing, Donald Reay, 2e,Wiley India Publication

REFERENCES

1. Digital Signal Processing Implementation using the TMS320C6000 DSP Platform, 1st Edition; Naim Dahnoun
2. Digital Signal Processing - A Student Guide,1st Edition; T.J. Terrel and Lik-Kwan Shark; Macmillan Press Ltd.
3. Digital Signal Processing: A System Design Approach, 1st Edition; David J Defatta J, Lucas Joseph G & Hodkiss William S ; John Wiley
4. Digital Signal Processing-A Practical Guide for Engineers and Scientists by Steven K Smith, Newnes, An imprint of Elsevier Science
5. DSP Applications using 'C' and the TMS320C6X DSK, 1st Edition; RulphChassaing
6. Digital Signal Processing Design, 1st Edition, Andrew Bateman, Warren Yates

NPTEL/ OTHER VIDEO RESOURCES

INTERNAL ASSESSMENT: 40 MARKS

Assessment procedure:

Two internal tests, each having 15%

Tutorials/Assignments/ Mini projects having 10%

End Semester examination having 60%

Module	COURSE PLAN Contents	Contact hours	Semester Exam Marks (%)
I	Introduction to a popular DSP from Texas Instruments, CPU Architecture, Functional Units, CPU Data Paths and Control, Internal Data/ Program Memory	7	15%
II	External Memory Interface, Timers, Interrupts, Pipelining, EDMA, Multi Channel Buffered Serial Port, Linear and Circular addressing	7	15%
	INTERNAL TEST 1		
III	Programming: Instruction Set and Addressing Modes, TMS 320C 64X /67X CPU Simple programming examples (Convolution, Dot product) using C, Linear Assembly and assembly language programming. Typical DSP development system, support tools and files, compiler, assembler, Code composer studio, CODECs, Typical DSP Development Kit	7	15%
IV	DSP Applications: Typical CODEC architecture, Sine wave generation from table data, DTMF Tone Generation and Detection Techniques and Implementation, Voice detection and reverse playback	7	15%
	INTERNAL TEST 2		
V	Digital Signal Processing Applications: Filter Design: FIR & IIR Digital Filter Design programs using MATLAB Fourier Transform: DFT, FFT programs using MATLAB Implementation of Real-time Digital filters using DSP: Implementation of FFT applications using DSP	7	20%
VI	RTDX between MATLAB and Code Composer Studio, DSP Controllers: Features of DSP controllers, peripherals (TMS 320 28XX series) Typical Architecture of DM 64XX series DaVinci SoC processor, Current Trends in Digital Signal Processors.	7	20%

Course code	Course Name	L-T-P-Credits	Year
07EC6606	**EMBEDDED AND REAL-TIME OPERATING SYSTEMS**	**3-0-0-3**	**2020**
Pre-requisite(s)	Basic Knowledge of C and assembly programming	Total Hours :42	

COURSE OBJECTIVES

- To provide a thorough understanding of Real-time kernel internals of embedded operating systems
- Understand the implementation techniques of a simple RTOS with the help of μC/ OS-II

SYLLABUS

Introduction to Real-time Concepts – Kernel Structure – Task Management in OS – Time Management – Event Control Blocks – Semaphore Management – Mutual Exclusion Semaphores – Event Flag Management – Message Mailbox Management – Message Queue Management – Memory Management – Porting of μC/ OS-II to other processors

COURSE OUTCOME

On completion of the course the student will be able to

1. Explain the important components and concepts to be implemented in a Real-time system
2. Explain and implement different process scheduling algorithms
3. Implement Task Management and Event Control operations in RTOS
4. Implement Deadlock management using semaphores and mutually exclusive locks
5. Implement Message passing between tasks using mail box
6. Explain the Memory Management and Queue Management Techniques

TEXT BOOKS

1. Jean J. Labrosse, "MicroC/OS-II The Real-time Kernel" Second Edition, CMP Books
2. Jim Cooling, Real-Time Operating Systems: Book 2 - The Practice: Using STM Cube, Free RTOS and the STM32 Discovery Board (2nd Edition Lindentree Associates 2020)
3. David E.Simon, "An Embedded Software Primer", Addison Wesley; Pap/Cdr edition (5 August 1999) 2nd Edition

REFERENCES

1. K.C.Wang, "Embedded and Real-Time Operating Systems", Springer; 1st ed. 2017 edition (6 April 2017)
2. Jean J. Labrosse, "µC/OS-III The Real-Time Kernel", Micrium (1 September 2009)
3. https://doc.micrium.com/display/osiidoc

NPTEL/ OTHER VIDEO RESOURCES

INTERNAL ASSESSMENT: 40 MARKS

Assessment procedure:

Two internal tests, each having 15%

Tutorials/Assignments/ Mini projects having 10%

End Semester examination having 60%

Module	COURSE PLAN Contents	Contact hours	Semester Exam Marks (%)
I	Introduction to Real-time Concepts – Foreground/Background systems – Critical Section - Shared resources – Multitasking – Tasks - Context Switches – Kernels – Schedulers – Preemptive/Non-Preemptive Kernels – Reentrant Functions – Round Robin Scheduling – Static/Dynamic Priorities – Priority Inversion – Priority Ceiling Deadlock - Synchronization – Event Flags - Intertask Communication – Message Mailbox – Message Queues Interrupts – Latency – Response - Recovery – ISR processing time-Non-maskable Interrupts - Clock Tick-memory requirements-Advantages of Real-time Kernels	7	15%
II	Concept of Real-time Operating Systems – Task Scheduling Algorithms – Rate Monotonic Scheduling – Earliest Deadline First – Deadline Monotonic – Survey of RTOS – FreeRTOS - µC/OS-II: µC/OS-II: Kernel Structure – Task State - Task Scheduling – Idle/Static Tasks – Interrupts - Clock Tick	7	15%
	INTERNAL TEST 1		
III	µC/OS-II : Task Management – Task Stacks – Priorities - functions for Task Management - Time Management – Time management operations µC/OS-II : Event Control Block – operations in ECB	7	15%

IV	Semaphore Management – Operations on Semaphores - Mutual Exclusion Semaphores – Mutex Functions µC/OS-II : Event Flag Management – Event Flag Group – manipulating using Event Flags	7	15%
	INTERNAL TEST 2		
V	Message Mailbox management – Operations on Mailbox – Using Mailbox as a Binary Semaphore – Mailbox for Time delay operation µC/OS-II : Message Queue Management – Operations in Message Queues –Message queue to read a Analog inputs – Using Queue as a counting semaphore	7	20%
VI	Memory Management – Memory Control Block – Operations Using Memory Partitions – Waiting for Memory Block from a Partition Porting µC/OS-II to other Processors	7	20%
	END SEMESTER EXAMINATION		

Course code	Course Name	L-T-P-Credits	Year
07EC6628	**NANO-SCALE DEVICES**	**3-0-0-3**	**2020**
Pre-requisite(s)	Nanoelectronics	Total Hours :42	

COURSE OBJECTIVES

- To understand the physics and effects of nanoscale multi-gate transistors in detail.
- To understand the concepts of Carbon Nanotube FETs & SETs.
- To familiarize with Graphene Technology & GFETs

SYLLABUS

Review of MOSFETS & Introduction to Nanoscale effects: MOSFET physics & I-V Characteristics-MOSFET Scaling & penalties. Nanoscale Effects: Gate Oxide leakage currents: Gate Oxide Tunneling & Impact-Models for QMDT in Gate Oxides Tunneling in Multiple Gate MOSFETs; Inversion Layer Quantization- Dielectrics for Nano electronics; The SOI MOSFET; Multi-gate MOSFET Technology; Physics of Multi-gate MOS system, Transistor Models- Mobility in Multi-gate MOSFETs-Double Gate MOSFETS & FinFETs; Radiation effects in Single &Multi-gate SOI MOSFETs- Multi-gate MOSFET circuit Design: Digital circuit design-Analog circuit design; Nanowire FETs: Silicon Nanowire MOSFETs-Carbon Nanotubes- Carbon nanotube FETs &MOSFETs; Transistors at molecular scale: Model for Ballistic Nanotransistors-MOSFETs with 0D,1D & 2D channels-Molecular Transistors-Single Electron Transistors.

COURSE OUTCOME

On completion of the course the student will be able to

1. Understand the concepts of different types of nanoscale transistors & the factors affecting it.
2. Familiarize the GFETs & the challenges facing in current Graphene technology.

TEXT BOOKS

1. J P Colinge, "FINFETs and other multi-gate transistors", Springer – Series on integrated circuits and systems, 2008.
2. Amit Chaudhry, "Fundamentals of Nanoscaled Field Effect Transistors", Springer, 2013.

REFERENCES

1. Mark Lundstrom Jing Guo, "Nanoscale Transistors: Device Physics, Modeling and Simulation", Springer, 2006.
2. Raghu Murali, "Graphene Nanoelectronics: From Materials to Circuits", Springer, 2012.

NPTEL/ OTHER VIDEO RESOURCES

INTERNAL ASSESSMENT: 40 MARKS

Assessment procedure:

Two internal tests, each having 15%

Tutorials/Assignments/ Mini projects having 10%

End Semester examination having 60%

Module	COURSE PLAN Contents	Contact hours	Semester Exam Marks (%)
I	Review of MOSFETS & Introduction to Nanoscale effects: MOSFET physics & I-V Characteristics-MOSFET Scaling-Penalties of scaling. Nanoscale Effects: Gate Oxide leakage currents: Gate Oxide Tunneling & Impact-Models for QMDT in Gate Oxides-Impact of parameters on QMDT current density-Tunneling in Multiple Gate MOSFETs; Inversion Layer Quantization: Inversion Layer Quantization in substrate- Modeling approaches-Existing models-Effect on Threshold voltage & Drain current; Dielectrics for Nanoelectronics.	6	15%
II	The SOI MOSFET: Brief History of Multiple-Gate MOSFETs, Multi-gate MOSFET physics. Multi-gate MOSFET Technology: Active area-Fins, - Gate stack-Source/Drain resistance & capacitance-Mobility & Strain engineering-Contacts to the Fins.	7	15%
	INTERNAL TEST 1		
III	Physics of Multi-gate MOS system, Transistor Models: Device electrostatics-Double Gate MOS system-2D confinement; A brief study on Multi-gate Transistor models-BSIM-CMG & BSIM-IMG; Mobility in Multi-gate MOSFETs: Double Gate MOSFETS &FinFETS: Photon limited mobility-interface roughness & coulomb scattering-Temperature dependence on mobility-high-k dielectrics; Silicon Multiple-gate Nanowires.	7	15%

IV	Radiation effects in Single &Multigate SOI MOSFETs: Total Ionizing Dose effects-Single Event effects. Multigate MOSFET circuit Design: Digital circuit design-Analog circuit design.	8	15%
	INTERNAL TEST 2		
V	Nanowire FETs : Silicon Nanowire MOSFETs-Carbon Nanotubes-Band structure of carbon nanotubes-Carbon nanotube FETs & MOSFETs- Schotkey barrier Carbon Nanotube FETs. Transistors at molecularscale: Electron conduction in molecules-Model for Ballistic Nanotransistors-MOSFETs with 0D,1D & 2D channels-Molecular Transistors-Single Electron Transistors.	8	20%
VI	Graphene Technology & GFETs: Evolution of Graphene Technology-Electronic transport in Graphene-Technical Challenges in GFETs graphene Transistors-Formation of Epitaxial Graphene- Graphene Growth by CVD methods-Graphene FET Models.	6	20%
	END SEMESTER EXAMINATION		

Course code	Course Name	L-T-P-Credits	Year
07EC6638	**CUSTOM DIGITAL CMOS SYSTEM DESIGN**	**3-0-0-3**	**2020**
Pre-requisite(s)	Digital Integrated Circuit Design	Total Hours :42	

COURSE OBJECTIVES

- To provide rigorous foundation in digital system level design methodologies and different subsystems used for custom design.

SYLLABUS

MOS Transistor Theory, CMOS Processing Technology, Delay, Power, Combinational Circuit Design, Sequential Circuit Design, Data-path Subsystems, Array Subsystems, Special-Purpose Subsystems, Design Methodology and Tools, Testing, Debugging, and Verification.

COURSE OUTCOME

On completion of the course the student will be able to

1. Understand Delay and Power inside Digital Integrated Circuits
2. Understand efficient combinational/sequential circuits.
3. Understand design options for common data-path operators.
4. Understand design options for Array Subsystems.
5. Understand design options for Special-Purpose Subsystems.
6. Understand different Design Methodology and Tools.

TEXT BOOKS

1. Neil H.E. Weste and David Money Harris, "CMOS VLSI Design-A Circuits and Systems Perspective", Pearson Education.

REFERENCES

1. Rabaey, Chandrakasan and Nikolic, "Digital Integrated Circuits – A Design Perspective", 2/e, Pearson Education.
2. R. Jacob Baker, Harry W. Li, David E. Boyce, "CMOS, Circuit Design, Layout, and Simulation", 3/e, Wiley Interscience.
3. John P.Uyemura "Introduction to VLSI Circuits and Systems", John Wiley & Sons, Inc., 2002.
4. Sung-Mo Kang, Yusuf Leblebici, "CMOS Digital Integrated Circuits-Analysis and Design", 3/e, Tata McGraw-Hill Education,2003.

NPTEL/ OTHER VIDEO RESOURCES

INTERNAL ASSESSMENT: 40 MARKS

Assessment procedure:

Two internal tests, each having 15%

Tutorials/Assignments/ Mini projects having 10%

End Semester examination having 60%

Module	COURSE PLAN Contents	Contact hours	Semester Exam Marks (%)
I	**MOS Transistor Theory: Review:** **CMOS Processing Technology:** CMOS Technologies, Layout Design Rules, CMOS Process Enhancements, Technology-Related CAD Issues, Manufacturing Issues. **Delay:** Transient Response, RC Delay Model, Linear Delay Model, Logical Effort of Paths, Timing Analysis Delay Models **Power:** Dynamic Power, Static Power, Energy-Delay Optimization, Low Power Architectures	7	15%
II	**Combinational Circuit Design:** Circuit Families, Circuit Pitfalls, Silicon-On-Insulator Circuit Design, Sub-threshold Circuit Design Sequential Circuit Design: Sequencing Static Circuits, Circuit Design of Latches and Flip-Flops, Static Sequencing Element Methodology, Sequencing Dynamic Circuits, Synchronizers, Wave Pipelining.	7	15%
	INTERNAL TEST 1		
III	**Data-path Subsystems:** Introduction, Addition/ Subtraction, One/Zero Detectors, Comparators, Counters, Boolean Logical Operations, Coding, Shifters, Multiplication, Parallel-Prefix Computations.	7	15%

IV	**Array Subsystems:** SRAM, DRAM, Read-Only Memory, Serial Access Memories, Content-Addressable Memory, Programmable Logic Arrays, Robust Memory Design.	7	15%
	INTERNAL TEST 2		
V	**Special-Purpose Subsystems:** Packaging and Cooling, Power Distribution, Clocks, PLLs and DLLs, I/0, High-Speed Links, Random Circuits.	7	20%
VI	**Design Methodology and Tools:** Structured Design Strategies, Design Methods, Design Flows, Design Economics, Data Sheets and Documentation, CMOS Physical Design Styles **Testing, Debugging, and Verification:** Testers, Test Fixtures, and Test Programs, Logic Verification Principles, Silicon Debug Principles, Manufacturing Test Principles, Design for Testability, Boundary Scan.	7	20%
	END SEMESTER EXAMINATION		

Course code	Course Name	L-T-P-Credits	Year
07EC6648	**IoT ARCHITECTURE AND PROTOCOLS**	**3-0-0-3**	**2020**
Pre-requisite(s)	Nil	Total Hours :42	

COURSE OBJECTIVES

- To familiarize students with the different IoT Architectures
- To provide a deep understanding on the communication protocols used in IoT implementations

SYLLABUS

IoT Architecture – Sensors and Actuators - Wireless Protocols – Data Protocols – IoT Programming – Arduino – Raspberry Pi – Reliability and Security issues in IoT – Big Data Analytics for IoT.

COURSE OUTCOME

On completion of the course the student will be able to

1. Explain and Classify the different IoT architectures
2. Explain the working of different wireless protocols used in IoT
3. Classify the different Data protocols used in IoT implementations
4. Write programs for Arduino and Raspberry Pi platforms for sensing applications
5. Explain the different reliability and security issues related to an IoT implementation
6. Recognize the use of Cloud computing for IoT implementation

TEXT BOOKS

1. Internet of Things: Principles and Paradigms –Rajkumar Buyya, Amir Vahid Dastjerdi.
2. Internet of Things for Architects: Architecting IoT solutions –Perry Lea
3. Marco Schwartz, "Internet of Things with Arduino Cookbook",Packt Publishing Limited,UK, 2016.
4. Peter Waher, "Learning Internet of Things", Packt Publishing Limited,UK,2015.
5. Arshdeep Bahga, Vijay Madisett, “Internet of Things: A Hands-On Approach”, VPT, 2014.

REFERENCES

1. Jan Holler, Vlasios Tsiatsis, Catherine Mulligan, Stamatis Karnouskos, David Boyle, "From Machine-to-Machine to the Internet of Things: Introduction to a New Age of Intelligence", Academic Press, USA, 2014.
2. Olivier Hersent, David Boswarthick, Omar Elloumi, "The Internet of Things: Key Applications and Protocols", Wiley, USA, 2012.

NPTEL/ OTHER VIDEO RESOURCES

INTERNAL ASSESSMENT: 40 MARKS

Assessment procedure:

Two internal tests, each having 15%

Tutorials/Assignments/ Mini projects having 10%

End Semester examination having 60%

Module	COURSE PLAN Contents	Contact hours	Semester Exam Marks (%)
I	Architecture: Physical Design -Logical Design, Enabling Technologies, IoT and M2M,SDN and NFV, IoT system management with NETCONF-YANG, Sensors and actuators, IoT Gateways, IT/OT integration	7	15%
II	Protocols: Infrastructure-6LowPAN-RPL -OPC, Identification-uCode -EPC, RF - Communication -Bluetooth -ZigBee -zwave -LPWAN, LoRaWAN, Discovery -mDNS -DNS -SD	7	15%
	INTERNAL TEST 1		
III	Data Protocols: REST -MQTT -CoAP, Device Management -TR-069, Semantic - JSON-LD -Web Thing Model, Multi-layer Frameworks – lljoyn	7	15%
IV	Programming in IoT: Arduino –Architecture -Programming, Interfacing sensors with Arduino, Reading data from sensors, Connecting Arduino with mobile devices, Raspberry Pi, Programming Raspberry Pi with Python, Thing Worx platform, CaseStudy: Home automation.	7	15%
	INTERNAL TEST 2		

V	Reliability and security issues in IoT: IoT Reliability, Security, Privacy and Governance, Robustness and Reliability: Characteristics and reliability issues, addressing reliability, Security and Privacy: Concepts, security overview, frameworks and privacy in IoT networks, IoT Governance Models and Issues	7	20%
VI	Big data analytics for IoT: IoT Cloud Platform: Data retrieval and Visualization, Fog Computing, Security, Privacy and Trust, Case Study: Smart Cities, Smart Logistic sand Retail, Agriculture, Pollution Control, Health and Lifestyle.	7	20%
	END SEMESTER EXAMINATION		

Course code	Course Name	L-T-P-Credits	Year
07EC6658	**AUTOMOTIVE EMBEDDED SYSTEMS**	**3-0-0-3**	**2020**
Pre-requisite(s)	UG level Understanding of Basics Control Theory and Discrete Time Systems, Basic electronic circuits and microprocessors.	Total Hours :42	

COURSE OBJECTIVES

- Understand the design of a complex system through the integration of various sub-systems
- Explain the working of critical sub systems of a modern day automobile

SYLLABUS

Use of Electronic in Vehicles – Basics of Electronic Engine Control – Sensors and Actuators Used in Automobiles – Digital Power train Control Systems – Comfort and Control Systems – Signaling and Vision – Vehicle Dynamic Safety – Driver and Passenger Safety – Diagnostic Techniques

COURSE OUTCOME

On completion of the course the student will be able to

1. Provide a basic understanding of Electronic Engine Control and their implementation in modern automobiles
2. Explain the principle and application of different sensors and actuators used in Automobiles
3. Explain the working of an Integrated Engine Control Unit and its different modes of operation
4. Explain the working of different user comfort and control systems in an automobile
5. Describe various user safety systems and their working
6. Introduce industry standard Multiplexed Networks for Embedded Systems

TEXT BOOKS

1. William Ribbens, "Understanding Automotive Electronics – An Engineering Perspective", Seventh Edition, Butterworth Heinemann, 2017
2. W. Hillier and David R. Rogers, "Hillier's Fundamentals of Motor Vehicle Technology, Book 3 – Chassis and Body Electronics", 5/e, Nelson Thornes Ltd, 2007
3. Dominique Paret, "Multiplexed Networks for Embedded Systems: CAN, LIN, FlexRay, Safe–by–Wire", First Edition, Wiley, 2007

REFERENCES

1. Behrooz Mashadi and David Crolla "Vehicle Power Train Concepts", John Wiley and Sons, 1st Edition
2. Tom Denton, "Automobile Electrical and Electronic Systems", Fourth Edition, Routledge, 2012
3. Edited by David A. Crolla, "Automotive Engineering Power train, Chassis System and Vehicle Body", First Edition, Butterworth Heinemann,2009

NPTEL/ OTHER VIDEO RESOURCES

INTERNAL ASSESSMENT: 40 MARKS

Assessment procedure:

Two internal tests, each having 15%

Tutorials/Assignments/ Mini projects having 10%

End Semester examination having 60%

Module	COURSE PLAN Contents	Contact hours	Semester Exam Marks (%)
I	Vehicle Power Train Concept - Engine Control Unit – Concept of Electronic Engine Control System – Exhaust Catalytic Converters – Electronic Fuel Control System –Idle Speed Control Electronic Ignition Automotive Control System Applications of Sensors and Actuators – Sensors: Throttle Angle - Temperature – Coolant – Knock	8	15%
II	Automotive Engine Control Actuators – Variable valve Timing – Electric Motor Actuators – Brushless DC motor – Ignition System Digital Engine Control – Features – Control Mode for Fuel Control – Discrete Time Idle Speed Control	8	15%
	INTERNAL TEST 1		
III	EGR Control – Variable Valve Timing Control – Electronic Ignition Control – Integrated Engine Control System – Control modes of Digital Engine Control System – Hybrid Electric Vehicle Power Train Control	7	15%

IV	Comfort and Control Systems: HVAC – Climate Control – Engine Cooling –Vehicle Security – Central Locking – Immobiliser Signalling And Vision : Light Sources – Halogen Bulbs – LEDs – Lamp Assemblies – Headlamp Levelling – Visual Signalling – Turn Signal Lamps – Flashers - Screens : - Wiper Assembly – Operation Modes – Washers	7	15%
	INTERNAL TEST 2		
V	Vehicle Dynamic Safety: Anti-lock Brake System – Traction Control System – Electronic Stability Program – Electronic Hydraulic Brakes Airbags – Seatbelt Tensioners.	6	20%
VI	Multiplexed Networks for Embedded Systems – CAN – Introduction – Physical Layer – Medium – High Speed and Low Speed CAN – Components, Application and Tools for CAN – TTCAN LIN – Local Interconnect Network – Basic Concept -	6	20%
	END SEMESTER EXAMINATION		

Course code	Course Name	L-T-P-Credits	Year
07EC6668	**EMBEDDED PRODUCT DEVELOPMENT**	**3-0-0-3**	**2020**
Pre-requisite(s)	Nil	Total Hours :42	

COURSE OBJECTIVES

- To provide better understanding on embedded product development process flows
- To introduce various product development approaches
- To familiarize Product prototyping, Testing, Benchmarking perspectives
- To familiarize various Industrial Design Strategies and introduce the concept of reverse engineering
- To familiarize how to select Software and Hardware components, development platforms, bus communication standards processors, memory ADC and various debugging tools etc
- To impart the need of Cost estimation, Product branding and documentation in development process flow

SYLLABUS

Concepts of product development: Five Step Method-Basics of Concept selection Creative thinking, Product development management - Architecture competitive benchmarking- Design for manufacturing - Industrial Design- Prototype, Testing Methodologies–-case study on Embedded product modeling- Selection of Sensor, Grounding and noise elimination methods, Thermal protection with heat management –

PCB design steps – Software design and testing method – Architectural Structures, processors, input/output interfaces & connectors, ADC System, Memory, choosing Bus Communication Standards, Embedded OS/Device Drivers, Translation & Debugging Tools & Application Software, Performance Testing, Costing, Benchmarking, Documentation

COURSE OUTCOME

On completion of the course the student will be able to

1. Understand the integration of customer requirements in product design
2. Apply structural approach to concept generation, creativity, selection and testing
3. Understand various aspects of design such as industrial design, design of Consumer specific products etc
4. Understand the need of benchmarking, Product branding, economic analysis
5. Understand the and product architecture and the concepts of Reverse Engineering
6. Involve Discussions/ Practice/Exercise onto revising & familiarizing the concepts acquired over the 6 Units of the subject for improved employability skills

TEXT BOOKS

1. "Product Design and Development", Anita Goyal, Karl T Ulrich, Steven D Eppinger, McGraw –Hill International Edns.1999/ Tata McGrawEducation, ISBN-10-007-14679
2. R.G. Kaduskar and V.B. Baru, " Electronic Product Design", Wiley, 2014
3. George E.Dieter, Linda C.Schmidt, "Engineering Design", McGraw-Hill International Edition,4th Edition, 2009, ISBN 978-007-127189-9
4. Stephen Armstrong, Engineering and Product Development Management ; The Holistic Approach, CAMBRIDGE UNIVERSITY PRESS (CUP),2014

REFERENCES

1. Rajkamal, 'Embedded system-Architecture, Programming, Design', TMH,2011.
2. Kevin Otto & Kristin Wood, "Product Design and Development", 4th Edition,2009, Product Design Techniques in Reverse Engineering and New Product Development,, Pearson Education (LPE),2001./ISBN 9788177588217
3. Yousef Haik, T. M. M. Shahin, "Engineering Design Process", 2nd Edition Reprint, Cengage Learning, 2010, ISBN 0495668141
4. Clive L.Dym, Patrick Little, "Engineering Design: A Project-based Introduction", 3rd Edition, John Wiley & Sons, 2009, ISBN 978-0-470-22596-7

Module	COURSE PLAN Contents	Contact hours	Semester Exam Marks (%)
I	Need for PD- Generic product Development Process Phases- Product Development Process Flows Product Development organization structures-Strategic importance of Product Planning process – Product Specifications-Target Specifications-Plan and establish product specifications - integration of customer, designer, material supplier and process planner, Competitor and customer – Understanding customer and behavior analysis.	7	15%
II	Concept Generation, Five Step Method-Basics of Concept selection Creative thinking –creativity and problem solving- creative thinking methods- generating design concepts-systematic methods for designing –functional decomposition – physical decomposition	5	15%
	INTERNAL TEST 1		
III	Product development management - establishing the architecture - creation - Product Architecture changes - variety – component standardization, clustering - geometric layout development - Fundamental and incidental interactions - related system level design issues - secondary systems - architecture of the chunks - creating detailed interface specifications-Portfolio Architecture competitive benchmarking- Approach for the benchmarking process-Design for manufacturing - Industrial Design-Robust Design – Prototype basics - Principles of prototyping - Planning for prototypes-Economic & Cost Analysis -Testing Methodologies-Product Branding	7	15%

IV	Role of Integrating CAE, CAD, CAM tools for Simulating product performance and manufacturing processes electronically- Basics on reverse engineering – Reverse engineering strategies – Finding reusable software components – Recycling real-time embedded software based approach and its logical basics- Incorporating reverse engineering for consumer product development – case study on DeskJet Printer	5	15%
	INTERNAL TEST 2		
V	Product Development Stages-Embedded product modeling- Linear, Iterative, Prototyping, Spiral - Selection of Sensor, Voltage Supply, Power supply protection, Grounding and noise elimination methods, Thermal protection with heat management – PCB design steps – Software design and testing method – documentation.	9	20%
VI	Creating general Embedded System Architecture(with Case study example: Mobile Phone / DeskJet Printer./ Robonoid as a product) -Architectural Structures- Criteria in selection of Hardware & Software Components, processors, input/output interfaces & connectors, ADC System, Memory, choosing Bus Communication Standards, Criteria in selection of Embedded OS/Device Drivers, Need for Developing with IDE, Translation & Debugging Tools & Application Software, Performance Testing, Costing, Benchmarking, Documentation	9	20%
	END SEMESTER EXAMINATION		

Course code	Course Name	L-T-P-Credits	Year
07EC6612	**VLSI DESIGN AUTOMATION**	**3-0-0-3**	**2020**
Pre-requisite(s)	Basic VLSI course	Total Hours :42	

COURSE OBJECTIVES

- To equip the students to model circuits using graphs.
- To enable the students to explain the basics of layout.
- To enable the students to solve problems in placement and partitioning tasks
- To familiarize students on the role of floor planning and optimization
- To equip students to apply Mapping of routing problems into graph domain.

SYLLABUS

Graph Algorithms, Logic Synthesis, High Level Synthesis, Compaction, Partitioning, Placement, Floor planning

COURSE OUTCOME

On completion of the course the student will be able to

1. Model circuits using graphs.
2. Explain the basics of layout and relevant design rules.
3. Recognize placement and partitioning stages apply algorithms to solve problems in those tasks
4. Describe role of floor planning and optimization
5. Apply Mapping of routing problems into graph domain
6. Describe high level synthesis

TEXT BOOKS

1. S.H. Gerez, "Algorithms for VLSI Design Automation", John Wiley & Sons, 2002.
2. N.A. Sherwani, "Algorithms for VLSI Physical Design Automation", Kluwer Academic Publishers,

REFERENCES

1. Meinel, Christoph, and Thorsten Theobald, "Algorithms and DataSstructures in VLSI Design: OBDD-Foundations and Applications",Springer-Verlag Berlin Heidelberg, 1998.
2. Drechsler, Rolf, "Evolutionary Algorithms for VLSI CAD" Springer Science & Business Media, 1998. 3. Trimberger, Stephen M., "An Introduction to CAD for VLSI", Springer Science & Business Media, 1987.
3. Sadiq M. Sait and H. Youssef, "VLSI Physical Design Automation: Theory and Practice", World Scientific, 1999.
4. Cormen, Thomas H., Charles E. Leiserson, and Ronald L. Rivest. "Introduction to Algorithms." The MIT Press, 3rd edition, 2009.

NPTEL/ OTHER VIDEO RESOURCES

INTERNAL ASSESSMENT: 40 MARKS

Assessment procedure:

Two internal tests, each having 15%

Tutorials/Assignments/ Mini projects having 10%

End Semester examination having 60%

Module	COURSE PLAN Contents	Contact hours	Semester Exam Marks (%)
I	Evolution of CAD tool-Importance of Design automation-Gate level Modeling-Higher levels of modeling-Review of Data structures and algorithms	7	15%
II	VLSI Design automation tools - Algorithmic Graph Theory and Computational Complexity – Tractable and Intractable problems - general purpose methods for combinatorial optimization.	7	15%
	INTERNAL TEST 1		
III	Layout Compaction - Design rules - problem formulation - algorithms for constraint graph compaction -	7	15%
IV	Placement and partitioning - Circuit representation - Placement algorithms – partitioning algorithms	7	15%
	INTERNAL TEST 2		
V	Floor planning concepts - shape functions and floor plan sizing - Types of local routing problems - Area routing - channel routing - global routing - algorithms for global routing.	7	20%
VI	High level Synthesis - Hardware models - Internal representation - Allocation assignment and scheduling - Simple scheduling algorithm - Assignment problem - High level transformations.	7	20%
	END SEMESTER EXAMINATION		

Course code	Course Name	L-T-P-Credits	Year
07EC6622	**TESTING OF VLSI CIRCUITS**	**3-0-0-3**	**2020**
Pre-requisite(s)	Degital circuit Design	Total Hours :42	

COURSE OBJECTIVES

- To enable the students to develop test patterns required to detect faults in a circuit
- To develop knowledge in the testability of a circuit
- To equip the students to design techniques to improve the testability of digital circuits.
- To enable the students to design Logic BIST circuits
- To able to explain Boundary scan architectures

SYLLABUS

Fault Modeling, Fault Simulation, Design for Testability, Test Generation, Built-In-Self-Test, Memory Testing, Boundary scan architectures

COURSE OUTCOME

On completion of the course the student will be able to

1. Develop test patterns required to detect faults in a circuit
2. Determine the testability of a circuit
3. Design methods/techniques to improve the testability of digital circuits.
4. Design Logic BIST circuits
5. Explain Boundary scan architectures

TEXT BOOKS

1. M. Abramovici, M.A. Breuer and A.D. Friedman, "Digital Systems and Testable Design", Jaico Publishing House, 2002.
2. P.K. Lala, "Digital Circuit Testing and Testability", Academic Press, 2002.
3. M.L. Bushnell and V.D. Agrawal, "Essentials of Electronic Testing for Digital,Memory and Mixed-Signal VLSI Circuits", Kluwer Academic Publishers, 2002.
4. A.L. Crouch, "Design Test for Digital IC's and Embedded Core Systems", Prentice Hall International, 2002.

REFERENCES

1. Wang Laung-Terng, Cheng-Wen Wu, and Xiaoqing Wen, VLSI test principles and architectures: design for testability, Academic Press, 2006.

NPTEL/ OTHER VIDEO RESOURCES

INTERNAL ASSESSMENT: 40 MARKS

Assessment procedure:

Two internal tests, each having 15%

Tutorials/Assignments/ Mini projects having 10%

End Semester examination having 60%

Module	COURSE PLAN Contents	Contact hours	Semester Exam Marks (%)
I	Introduction to Testing - Faults in digital circuits - Modeling of faults - Logical Fault Models – Fault detection - Fault location - Fault dominance - Logic Simulation - Types of simulation - Delay models - Gate level Event-driven simulation.	7	15%
II	Introduction, Exhaustive testing, Boolean difference, Basic ATPG algorithms sequential circuits - design of testable sequential circuits. ATPG for non stuck-at faults, Other issues in test generation	7	15%
	INTERNAL TEST 1		
III	Design for Testability: Introduction, Testability Analysis, DFT Basics, Scan cell design, Scan Architecture, Scan Design Rules-Scan Design Flow-Special purpose scan designs-RTL design for Testability	7	15%
IV	Built-In-Self-Test: Introduction, BIST design rules Test pattern generation, Output response analysis, Logic BIST architectures	7	15%
	INTERNAL TEST 2		
V	Boundary Scan-Digital Boundary scan-Boundary scan Architectures-TAP controller, EXTEST, INTEST, Boundary scan description language-SoC test problems and requirements-Test access mechanism architecture.	7	20%
VI	Memory Testing: Introduction, RAM fault models, RAM test generation. Memory BIST Power and Thermal Aware Test.	7	20%
	END SEMESTER EXAMINATION		

Course code	Course Name	L-T-P-Credits	Year
07EC6632	**DESIGN WITH ARM MICROCONTROLLERS**	**3-0-0-3**	**2020**
Pre-requisite(s)	Nil	Total Hours :42	

COURSE OBJECTIVES

- To impart embedded system design knowledge using the architecture and programming of Industry popular 32-bit Microcontroller - ARM Cortex

SYLLABUS

ARM Architecture, Cortex-M3 Basics, Exceptions, Instruction Sets, NVIC, Interrupt Behavior, Cortex-M3/M4 Programming, Exception Programming, Memory Protection Unit and other Cortex-M3 features, STM32L15xxx ARM Cortex M3/M4 Microcontroller Memory and Peripherals, Development & Debugging Tools

COURSE OUTCOME

On completion of the course the student will be able to

1. Understand the architecture and programming of Industry standard 32-bit popular ARM Cortex Microcontroller
2. Select a proper Microcontroller for a particular application
3. Understand the usage of the development and debugging tools
4. Write programs using ARM instruction set and appreciate the advanced features provided in ARM
5. Understand the features and application of ARM-Cortex-M3 processors

TEXT BOOKS

1. The Definitive Guide to the ARM Cortex-M3, Joseph Yiu, Second Edition, Elsevier Inc. 2010.
2. Dr.Yifeng Zhu, "Embedded Systems with ARM Cortex-M Microcontrollers in Assembly Language and C (Third Edition)" E-Man Press LLC; 3rd edition (July 2017)
3. Lyla B. Das, Embedded Systems – An Integrated Approach, Dorling Kindersley (India) Pvt. Ltd, licensees of Pearson Education in South Asia
4. Andrew N Sloss, Dominic Symes, Chris Wright, "ARM System Developer's Guide Designing and Optimizing System Software", 2006, Elsevier

REFERENCES

1. Steve Furber, "ARM System-on-Chip Architecture", 2nd Edition, Pearson Education
2. Cortex-M series-ARM Reference Manual
3. Cortex-M3 Technical Reference Manual (TRM)
4. Prasad, KVK, Embedded/Real-time Systems Concepts, Design and Programming Black Book,
5. David Seal "ARM Architecture Reference Manual", 2001 Addison Wesley, England; Morgan Kaufmann Publishers
6. Ajay Deshmukh, "Microcontroller - Theory & Applications", Tata McGraw Hill
7. Arnold. S. Berger, "Embedded Systems Design - An introduction to Processes, Tools and Techniques", Easwer Press
8. STM32L152xx ARM Cortex M3 Microcontroller Reference Manual
9. ARM Company Ltd. "ARM Architecture Reference Manual– ARM DDI 0100E"

NPTEL/ OTHER VIDEO RESOURCES

INTERNAL ASSESSMENT: 40 MARKS

Assessment procedure:

Two internal tests, each having 15%

Tutorials/Assignments/ Mini projects having 10%

End Semester examination having 60%

Module	COURSE PLAN Contents	Contact hours	Semester Exam Marks (%)
I	**ARM Architecture:** Background of ARM Architecture, Architecture Versions, Processor Naming, Instruction Set Development, Thumb-2 and Instruction Set Architecture. **Overview of Cortex-M3:** Cortex-M3 Basics: Registers, General Purpose Registers, Stack Pointer, Link Register, Program Counter, Special Registers.	6	15%
II	Operation Mode, Exceptions and Interrupts, Vector Tables, Stack Memory Operations, Reset Sequence. Instruction Sets: Assembly Basics, Instruction List, Instruction Descriptions.	8	15%
	INTERNAL TEST 1		
III	**Cortex-M3 Implementation Overview:** Pipeline, Block Diagram, Bus Interfaces on Cortex-M3, I-Code Bus, D-Code Bus, System Bus, External PPB and DAP Bus. **Exceptions:** Exception Types, Priority, Vector Tables, Interrupt Inputs and Pending Behaviour, Fault Exceptions, Supervisor Call and Pendable Service Call.	7	15%

IV	**NVIC:** Nested Vectored Interrupt Controller Overview, Basic Interrupt Configuration, Software Interrupts and SYSTICK Timer. **Interrupt Behaviour:** Interrupt/Exception Sequences, Exception Exits, Nested Interrupts, Tail-Chaining Interrupts, Late Arrivals and Interrupt Latency	7	15%
	INTERNAL TEST 2		
V	**Cortex-M3/M4 Microcontroller:** STM32L15xxx ARM Cortex M3/M4 Microcontroller: Memory and Bus Architecture, Power Control, Reset and Clock Control. **STM32L15xxx Peripherals:** GPIOs, System Configuration Controller, NVIC, ADC, Comparators, GP Timers, USART.	7	20%
VI	**Development & Debugging Tools:** Software and Hardware tools like Cross Assembler, Compiler, Debugger, Simulator, In-Circuit Emulator (ICE), Logic Analyzer etc.	7	20%
	END SEMESTER EXAMINATION		

Course code	Course Name	L-T-P-Credits	Year
07EC6642	**EMBEDDED LINUX SYSTEMS**	**3-0-0-3**	**2020**
Pre-requisite(s)	Operating system concepts	Total Hours :42	

COURSE OBJECTIVES

- To familiarize the students with Linux System in Embedded world and to provide a deep knowledge about the Development systems and files systems
- Enable the student to understand the concepts of using memory of the systems

SYLLABUS

Introduction: Types of Embedded Linux systems, Examples of Embedded Linux systems, Processor architectures supported by Linux; Cross platform Development tool chain: GNU tool chain basics, Bootstrap Compiler Setup, Using the tool chain, C library alternatives, Terminal Emulators; Kernel and Root File System: Kernel Considerations, Libraries, Kernel Modules, Kernel Images, Device Files, Main System Applications, System Initialization; Storage Device Manipulation; Root File system Setup; Setting Up the Boot loader; Device Drivers- Introduction, Building and running modules, Char Drivers, Allocating memory, USB Drivers, Device Model, Memory mapping and DMA, Block Drivers, TTY Drivers

COURSE OUTCOME

On completion of the course the student will be able to

1. Develop a strong understanding of using the tool chain.
2. Understand the concepts of file systems and device drivers.
3. Deploy a Linux operating systems in an appropriate embedded processors
4. Identify the requirements and apply it for developing a device driver in Linux
5. Identify the requirements and apply it for developing a USB based device driver in Linux

TEXT BOOKS

1. KarimYaghmour, JonJason Brittain and Ian F. Darwin Masters, Gilad Ben-Yossef, and Philippe Gerum, O'Reilly, Building Embedded Linux Systems 2nd Edition, 2008
2. Alessandro Rubini, Jonathan Corbet, O'Reilly, Linux Device Drivers, 3rd Edition, 2005

REFERENCES

1. Christopher Hallinan, Embedded Linux Primer A Prctical Real – World Approch, Prentice Hall.
2. P Raghavan, Amol Lad, SriramNeelakandan, Embedded Linux System Design and Development, Auerbach Publications.
3. Alan Cox, Sreekrishnan, Venkateswaran, Essential Linux Device Drivers, Pretice Hall.
4. Craig Hollabaugh, Embedded Linux Hardware, Software and Interfacing, Pearson Education.

NPTEL/ OTHER VIDEO RESOURCES

INTERNAL ASSESSMENT: 40 MARKS

Assessment procedure:

Two internal tests, each having 15%

Tutorials/Assignments/ Mini projects having 10%

End Semester examination having 60%

Module	COURSE PLAN Contents	Contact hours	Semester Exam Marks (%)
I	Introduction: Embedded Linux, Real-time Linux, Types of Embedded Linux systems, Advantages of Linux OS, Using distributions, Examples of Embedded Linux systems-system architecture, Types of host/target architectures for the development of Embedded Linux Systems, Debug setups, Boot Configurations, Processor architectures supported by Linux	7	15%
II	Cross platform Development Tool chain: GNU tool chain basics, Kernel Headers Setup, Binutils setup, Bootstrap Compiler Setup, Library Setup, Full Compiler Setup, Using the tool chain, C library alternatives, JAVA, Perl, Python, Ada, IDEs, Terminal Emulators	7	15%
	INTERNAL TEST 1		
III	Kernel and Root File System: Kernel Considerations-selection, configuration, Compiling and Installing the kernel Root File System Structure, Libraries, Kernel Modules, Kernel Images, Device Files, Main System Applications, Custom Applications, System Initialization	6	15%

IV	Storage Device Manipulation: MTD-Supported Devices, Disk Devices, Swapping. Root File system Setup :File system Types for Embedded Devices, Writing a File system Image to Flash using an NFS-Mounted Root File system, Placing a Disk File system on a RAM Disk, Rootfs and Initramfs, Choosing a Filesystem's Type and Layout, Handling Software Upgrades. Setting Up the Bootloader :Embedded Boot loaders, Server Setup for Network Boot, Using the U-Boot Boot loader	8	15%
	INTERNAL TEST 2		
V	Device Drivers-Part I: Introduction, Building and running modules, Char Drivers, Allocating memory.	7	20%
VI	Device Drivers-Part II: USB Drivers, Device Model, Memory mapping and DMA, Block Drivers, TTY Drivers.	7	20%
	END SEMESTER EXAMINATION		

Course code	Course Name	L-T-P-Credits	Year
07EC6652	**PRINCIPLES OF CO-DESIGN**	**3-0-0-3**	**2020**
Pre-requisite(s)	Nil	Total Hours :42	

COURSE OBJECTIVES

To impart knowledge on:

- Design steps starting from system specifications to hardware/software implementation
- Process optimization while considering various design decisions.

SYLLABUS

Introduction to Hardware/Software Co-design, Processor Synthesis, Single and Multi-processor Architecture, Partitioning Problem, Formulation of HW/SW portioning problem, Genetic Algorithms, Co-Synthesis Problem, Distributed System Co-synthesis, Prototyping and emulation, Target Architectures, Mixed Systems and Less Specialized Systems, Concurrency, Design representation of System level synthesis, System level Specification Languages

COURSE OUTCOME

On completion of the course the student will be able to

1. Outline and apply design methodologies
2. Appreciate the fundamental building blocks of using hardware and software co-design and related implementation and testing environments and techniques and their inter-relationships
3. Modern hardware/software tools for building prototypes
4. Demonstrate practical competence in these areas.

TEXT BOOKS

1. Ralf Niemann, "Hardware/Software Co-Design for Data Flow Dominated Embedded Systems", Kluwer Academic Pub, 1998. 2014.
2. Jorgen Staunstrup, Wayne Wolf, "Hardware/Software Co-Design: Principles and Practice", Kluwer Academic Pub,1997.
3. Giovanni De Micheli, Rolf Ernst Morgon," Reading in Hardware/Software Co-Design " Kaufmann Publishers,2001.

REFERENCES

NPTEL/ OTHER VIDEO RESOURCES

INTERNAL ASSESSMENT: 40 MARKS

Assessment procedure:

Two internal tests, each having 15%

Tutorials/Assignments/ Mini projects having 10%

End Semester examination having 60%

Module	COURSE PLAN Contents	Contact hours	Semester Exam Marks (%)
I	**System Specification And Modeling** : Embedded Systems, Hardware/Software Co-Design, Co-Design for System Specification and Modeling Co-Design for Heterogeneous Implementation - Processor Synthesis, Single- Processor Architectures with one ASIC, Single-Processor Architectures with many ASICs, Multi- Processor Architectures, Comparison of Co-Design Approaches, Models of Computation, Requirements for Embedded System Specification .	7	15%
II	**Hardware/Software Partitioning**: The Hardware/Software Partitioning Problem, Hardware-Software Cost Estimation, Generation of the Partitioning Graph, Formulation of the HW/SW Partitioning Problem, Optimization, HW/SW Partitioning based on Heuristic Scheduling, HW/SW Partitioning based on Genetic Algorithms.	7	15%
	INTERNAL TEST 1		
III	The Co-Synthesis Problem, State-Transition Graph, Refinement and Controller Generation, Distributed System Co-Synthesis	7	15%

IV	**Hardware/Software Co-Synthesis**: Introduction, Prototyping and Emulation Techniques, Prototyping and Emulation Environments, Future Developments in Emulation and Prototyping, Target Architecture- Architecture Specialization Techniques, System Communication Infrastructure, Target Architectures and Application System Classes, Architectures for Control-Dominated Systems, Architectures for Data- Dominated Systems, Mixed Systems and Less Specialized Systems	7	15%
	INTERNAL TEST 2		
V	**Prototyping And Emulation**: Introduction, Prototyping and Emulation Techniques, Prototyping and Emulation Environments, Future Developments in Emulation and Prototyping, Target Architecture- Architecture Specialization Techniques, System Communication Infrastructure, Target Architectures and Application System Classes.	7	20%
VI	Architectures for Control-Dominated Systems, Architectures for Data- Dominated Systems, Mixed Systems and Less Specialized Systems. **Design Specification And Verification**: Concurrency, Coordinating Concurrent Computations, Interfacing Components, Verification, Languages for System-Level Specification and Design System-Level Specification, Design Representation for System Level Synthesis, System Level Specification Languages, Heterogeneous Specification and Multi-Language Co-simulation	7	20%
	END SEMESTER EXAMINATION		

Course code	Course Name	L-T-P-Credits	Year
07EC6262	**HIGH SPEED DIGITAL SYSTEMS**	**3-0-0-3**	**2020**
Pre-requisite(s)	Basic course in Digital Electronics, Electromagnetic theory	Total Hours :42	

COURSE OBJECTIVES

- To acquaint the students with the problems associated with high-speed digital devices
- To provide an overview of power distribution and noise
- To study about timing and synchronization

SYLLABUS

Introduction to high speed digital design: Capacitance and inductance effects, High speed properties of logic gates, Speed and power, Modeling of wires, transmission, Power distribution and noise: Power supply network, local power regulation, IR, on chip bypass capacitors, power supply isolation, Noise sources in digital system, Signaling convention and circuits, Signaling modes for transmission lines, Driving lossy LC lines, simultaneous bi-directional signaling, Timing convention and synchronization, timing properties of clocked storage elements, pipeline timing, synchronization failure and meta-stability, PLL and DLL based clock aligners

COURSE OUTCOME

On completion of the course the student will be able to

1. Understand the design issues in high speed digital devices
2. Consider the different noise sources while designing a power distribution network
3. Appreciate the significance of timing and synchronization

TEXT BOOKS

1. Howard Johnson and Martin Graham, High Speed Digital Design: A Handbook of Black Magic, 3rd Edition, Prentice Hall Modern Semiconductor Design Series' Sub Series: PH Signal Integrity Library, 2006
2. Stephen H. Hall, Garrett W. Hall, and James A. McCall, High-Speed Digital System Design: A Handbook of Interconnect Theory and Design Practices, Wiley, 2007

REFERENCES

1. Kerry Bernstein, K.M. Carrig, Christopher M. Durham, and Patrick R. Hansen, High Speed CMOS Design Styles, Springer Wiley 2006
2. Ramesh Harjani, Design of High-Speed Communication Circuits (Selected Topics in Electronics and Systems), World Scientific Publishing Company, 2006

NPTEL/ OTHER VIDEO RESOURCES

INTERNAL ASSESSMENT: 40 MARKS

Assessment procedure:

Two internal tests, each having 15%

Tutorials/Assignments/ Mini projects having 10%

End Semester examination having 60%

Module	COURSE PLAN Contents	Contact hours	Semester Exam Marks (%)
I	Introduction to high speed digital design: Frequency, time and distance - Capacitance and inductance effects - High seed properties of logic gates - Speed and power	7	15%
II	Modelling of wires -Geometry and electrical properties of wires - Electrical models of wires -transmission lines - lossless LC transmission lines – lossy LRC transmission lines - special transmission lines	7	15%
	INTERNAL TEST 1		
III	Power distribution and noise: Power supply network - local power regulation - IR drops - area bonding - on chip bypass capacitors - symbiotic bypass capacitors - power supply isolation	7	15%
IV	Noise sources in digital system - power supply noise - cross talk – inter-symbol interference, Noise Budget design, Statistical Analysis	7	15%
	INTERNAL TEST 2		
V	Signalling convention and circuits: Signalling modes for transmission lines -signalling over lumped transmission media - signalling over RC interconnect –Driving lossy LC lines - simultaneous bi-directional signalling - terminations - transmitter and receiver circuits	7	20%
VI	Timing convention and synchronization, Timingfundamentals - timing properties of clocked storage elements - signals and events -open loop timing level sensitive clocking - pipeline timing - closed loop timing - clock distribution - synchronization failure and meta-stability - PLL and DLL based clock aligners	7	20%

Course code	Course Name	L-T-P-Credits	Year
07EC6614	**SEMINAR - I**	**0-0-2-2**	**2020**
Pre-requisite(s)	Nil	Total Hours :	

COURSE OBJECTIVES

This course is intended for

- Increasing the breadth of knowledge
- Enhancing the ability of self-study
- Improving presentation and communication skills
- Augmenting the skill of Technical Report Writing.

OUTLINE AND EVALUATION PROCEDURE

Students have to register for the seminar and select a topic in consultation with any faculty member offering courses for the programme. A detailed write-up on the topic of the seminar is to be prepared in the prescribed format given by the Department. The seminar shall be of 30 minutes duration and a committee with the Head of the department as the chairman and two faculty members from the department as members shall evaluate the seminar based on the report and coverage of the topic, presentation and ability to answer the questions put forward by the committee. Faculty member in charge of the seminar and another faculty member in the department nominated by the Head of the Department are the evaluators for the seminar.

Internal Assessment: 100 Marks

The distribution of marks for seminar is as follows

Marks for the report: 30%

Presentation: 40%

Ability to answer questions on the topic: 30%

COURSE OUTCOME

The graduate will have acquired

1. Debating capability and presentation skills in a technical topic of his interest.
2. Knowledge about contemporary issues and research opportunities
3. Capacity to communicate effectively and professionally in both verbal and written forms
4. Capability for self-education and lifelong learning.

Course code	Course Name	L-T-P-Credits	Year
07EC6616	**MINI PROJECT**	**0-0-4-2**	**2020**
Pre-requisite(s)	Nil	Total Hours :--	

COURSE OBJECTIVES

- To practice the steps involved for the selection, execution, and reporting of the project

OUTLINE AND EVALUATION PROCEDURE

Individual students are required to choose a topic of their interest in the field of VLSI and Embedded Systems. The subject content of the mini project shall be from emerging / thrust areas, topics of current relevance having research aspects. The final evaluation of mini project will be carried out by a committee consisting of three faculty members from the department. The students should bring the report duly authenticated by the respective guide. Students individually will present their work before the committee. The report complete in all respects should be submitted to the Head of the department.

Internal Assessment: 100 Marks

The distribution of marks for seminar is as follows

Report – 20%

Demonstration and presentation – 50%,

Results -30%

COURSE OUTCOME

The graduate will have acquired

1. Skills to select and execute projects.
2. Technical report writing skills.

Course code	Course Name	L-T-P-Credits	Year
07EC6618	**VLSI DESIGN LAB**	**0-0-2-1**	**2020**
Pre-requisite(s)	Nil	Total Hours : 28	

COURSE OBJECTIVES

- To enable the students to design & analyze digital and analog circuits in CMOS

TOOLS

CADENCE/SYNOPSYS/MENTOR GRAPHICS/MAGIC or any other equivalent tools.

COURSE OUTCOME

1. Design & analyze analog and digital circuits in CMOS
2. Design various circuits to satisfy the performance parameters of the design.
3. Draw the layout of digital and analog circuits

INTERNAL ASSESSMENT:100 MARKS

Assessment procedure:

i) Practical Records /outputs - 40%

ii) Regular Class Viva-Voce - 20%

iii) Final Test (Objective) - 40%

LIST OF EXPERIMENTS

PART A

Design (Schematic), Simulation and Characterization of the following CMOS Logic Circuits

1. Inverter
2. NAND
3. NOR
4. Adders
5. Flip-Flops

PART B

Schematic Design, Simulation and Characterization of the following Analog Circuits

1. OPAMP
2. Two - Stage OPAMP with CMFB
3. Comparator
4. 8 - Bit Current Steering DAC/ Charge Scaling DAC

MOSFET Device Characterization for Small Signal Device Parameters and Parasitics Design (Schematic and Layout), Simulation and Characterization of the following Analog Circuits.

1. Current Mirrors
2. Voltage Reference
3. Single Stage amplifier configurations
4. Common Source
5. Common Gate
6. Common Drain
7. Differential Amplifier

SEMESTER -3
SYLLABI

Course code	Course Name	L-T-P-Credits	Year
07EC7601	**MIXED SIGNAL INTEGRATED CIRCUIT DESIGN**	**3-0-0-3**	**2020**
Pre-requisite(s)	Analog Integrated Circuit Design	Total Hours :42	

COURSE OBJECTIVES

- To develop the ability to design and analyze t circuits.

SYLLABUS

Switched Capacitor Circuits, Switched Capacitor Integrators, z-Domain Models of Two-Phase Switched Capacitor Circuits D/A converter:, Static non-idealities and Dynamic non-idealities, A/D Converter: Static non-idealities and Dynamic non-idealities, First and Second Order and Multi-bit Sigma-Delta Modulators, Basics of PLL, Basics of Delay Locked Loops.

COURSE OUTCOME

On completion of the course the student will be able to

1. Explain Switched capacitor circuits.
2. Analyze the non-idealities of converter circuits and study various DAC circuits.
3. Understand various ADC circuits and modulator circuits.
4. Explain PLL, DLL and perform mixed-signal layout.
5. Explain Data transmission using current and voltage signaling.

TEXT BOOKS

1. Behzad Razavi, "Design of Analog CMOS Integrated Circuits", Tata Mc-Graw Hill.
2. Jacob Baker, "CMOS mixed-signal circuit design", Wiley India.
3. Paul R. Gray and Robert G.Meyer, "Analysis and Design of Analog Integrated Circuits", John Wiley & Sons.

REFERENCES

1. Alan B. Gnebene, "Bipolar and MOS analog integrated circuit design", John Wiley & Sons.
2. Mohammed I. Elmasy," Digital Bipolar circuits ", John Wiley & Sons.
3. Gregorian& Tames, "Analog Integrated Circuit For Switched Capacitor Circuit ", Wiley

NPTEL/ OTHER VIDEO RESOURCES

INTERNAL ASSESSMENT: 40 MARKS

Assessment procedure:

Two internal tests, each having 15%

Tutorials/Assignments/ Mini projects having 10%

End Semester examination having 60%

Module	COURSE PLAN Contents	Contact hours	Semester Exam Marks (%)
I	Continuous-Time Signal Processing-Sampled-Data Signal Processing. Switched Capacitor Circuits - Switched Capacitor Amplifiers- Switched Capacitor Integrators.	7	15%
II	z-domain Models of Two-Phase Switched Capacitor Circuits-First-Order Switched Capacitor Circuits Second-Order Switched Capacitor Circuits- Switched Capacitor Filters.	7	15%
	INTERNAL TEST 1		
III	D/A converter-General considerations. Static non-idealities and Dynamic non-idealities, Current – steering DAC-Binary weighted DAC, Thermometer DAC, Design issues, Effect of Mismatches	7	15%
IV	A/D Converter- General considerations. Static non-idealities and Dynamic non-idealities. Flash ADC-Basic architectures. Successive Approximation ADC. Dual Slope A/D Converters -Pipe Line ADC. Hybrid ADC structures. Nyquist rate A/D Converters- Modulators for over sampled A/D Conversion	7	15%
	INTERNAL TEST 2		
V	First and Second Order and Multi-bit Sigma - Delta Modulators - Interpolative Modulators – Cascaded Architecture - Decimation Filters. Basics of PLL. Analog PLL and Digital PLL Circuits	7	20%
VI	Basics of Delay Locked Loops. Mixed-signal layout, Interconnects and data transmission. Data transmission using voltage mode signaling and current mode signaling.	7	20%
	END SEMESTER EXAMINATION		

Course code	Course Name	L-T-P-Credits	Year
07EC7611	**EMERGING ARCHITECTURES FOR MACHINE LEARNING**	**3-0-0-3**	**2020**
Pre-requisite(s)	Nil	Total Hours :42	

COURSE OBJECTIVES

- To familiarize the students to the new paradigms in computing.
- To give an exposure to popular Cloud and IoT technologies.
- To introduce the students to the potential of FPGAs in neural networks and bioinformatics.
- To give exposure to designing systems using state of the art computing tools.

SYLLABUS

GPU, CUDA, Cloud and IoT, FPGA and Reconfigurable Architectures in Bioinformatics.

COURSE OUTCOME

On completion of the course the student will be able to

1. Design neural networks
2. Design high performance bioinformatics database analysis Systems.
3. Design solution for solving problems in a big data cloud environment.
4. Identify GPU based solutions for dataflow intensive problems.
5. Design efficient applications using IoT technologies.
6. Explain the potential of FPGAs in neural networks and bioinformatics.

TEXT BOOKS

1. David B. Kirk, Wen-Mei W. Hwu, Programming Massively Parallel Processors: A Hands-on Approach, Second Edition, Morgan Kauffman, 2016.
2. Bertil Schmidt, Bioinformatics: High Performance Parallel Computer Architectures, CRC Press, 2011.

REFERENCES

1. Amos R Omondi and Jagath C Rajapakse, FPGA Implementation of Neural Networks, Springer, 2006.
2. Arshdeep Bahga and Vijay Madisetti, Internet of Things A Hands on Approach, Published by the Authors, 2014.
3. Bishop, Christopher M. Machine learning and pattern recognition, Information Science and Statistics. Springer, Heidelberg, 2006.

NPTEL/ OTHER VIDEO RESOURCES

INTERNAL ASSESSMENT: 40 MARKS

Assessment procedure:

Two internal tests, each having 15%

Tutorials/Assignments/ Mini projects having 10%

End Semester examination having 60%

Module	COURSE PLAN Contents	Contact hours	Semester Exam Marks (%)
I	Heterogeneous parallel computing-Architecture of modern GPU-Parallel programming languages and Models- GPU computing-Scalable GPUs.	7	15%
II	Data parallelism, CUDA program structure, Device global memory and data transfer-kernel functions and threading-Open CL	7	15%
	INTERNAL TEST 1		
III	Case studies IoT and cloud architectures-VLSI design challenges for IoT-Power-Area-Security. Overview of cloud computing-Introduction to Hadoop Framework	7	15%
IV	Review of Neural Networks .Case studies- FPGA architecture for Neural networks, FPGA hardware for Bioinformatics.	7	15%
	INTERNAL TEST 2		
V	Data Precision and Implementation Issues – Case Studies of Regression Implementation	7	20%
VI	FPGA and Reconfigurable Architectures for Bioinformatics – Database Search in bioinformatics – Sequencing and Alignment.	7	20%
	END SEMESTER EXAMINATION		

Course code	Course Name	L-T-P-Credits	Year
07EC7621	**EMBEDDED APPLICATIONS IN POWER ELECTRONICS**	**3-0-0-3**	**2020**
Pre-requisite(s)	Nil	Total Hours :42	

COURSE OBJECTIVES

- To familiarize various semiconductor power devices
- To provide better understanding on Power converter design
- To familiarize gate driving schemes of MOSFET and IGBTs
- To familiarize the peripherals of dsPIC and study the features of Motor control PWM
- To familiarize the design considerations of inverters, UPS, and SMPSs
- To familiarize different battery technologies
- To impart the requirements of PFC, Protection and thermal management

SYLLABUS

Power semiconductor devices and applications, Power Converters, Practical Converter design considerations, Magnetic components, Design of controllers for Power converters, dsPIC 30f2010 features, PWM generation and ADC interface, Interfacing of controller output to power module, Battery technology – different battery charging schemes, Design of UPS, concept of PFC, MPPT, protection devices and magnetic components.

COURSE OUTCOME

On completion of the course the student will be able to

1. Understand the fundamental concepts of power converter design
2. Apply the design consideration for selection of magnetic components, switching components like MOSFET, IGBT etc, controllers and gate drives
3. Apply the basic equations and design considerations for the design of applications like dc-dc converters, ups, battery chargers etc.
4. Understand the fundamental concepts PFC, MPPT etc

TEXT BOOKS

1. Power Electronics; By: Mohan, Underland, Robbins; John Wiley & Sons
2. Simplified design of Switching Power supplies; By: John D Lenk; EDN series for designers

REFERENCES

1. Design of magnetic components for switched mode power converters; By L Umanad, S.R Bhat; Wiely Eastern ltd
2. MOSFET& IGBT Designers manual, International Rectifier,
3. UPS design guide, International Rectifier
4. https://batteryuniversity.com/learn/
5. http://ww1.microchip.com/downloads/en/devicedoc/70118e.pdf
6. Relevant data sheets and application notes provided by the manufacturers

NPTEL/ OTHER VIDEO RESOURCES

INTERNAL ASSESSMENT: 40 MARKS

Assessment procedure:

Two internal tests, each having 15%

Tutorials/Assignments/ Mini projects having 10%

End Semester examination having 60%

Module	COURSE PLAN Contents	Contact hours	Semester Exam Marks (%)
I	Power semiconductor devices – Power Diodes, BJT, MOSFET, IGBT.– ratings and SOA, Switching characteristics, Gate Charge, Paralleling devices. Requirements and characteristics of Gate driver circuits/modules for power MOSFETs and IGBTs & Design of turn on and turn off snubbers. Dead time control.	7	15%
II	Types to Power converters and Design considerations: Buck, Boost, Buck-boost SEPIC and CUK converters. Isolated and Non isolated converters. Design of Synchronous buck converter. Interfacing of controller output to power module. High side and low side gate drivers- Need of isolated gate drives. Dedicated gate driver ICs- TLP350.	7	15%
	INTERNAL TEST 1		
III	Introduction to dsPIC,- overview of peripheral features of dsPIC30f2010- Detailed study of Motor control PWM and ADC:- PWM output channels - Complementary or Independent Output modes - Edge and Center Aligned modes - duty cycle generators- Dedicated time base - Programmable output polarity - Dead time control for Complementary mode - Manual output control - Trigger for synchronized A/D conversions- 10 bit ADC	6	15%

IV	Inverters with square and sinusoidal output. PWM switching – unipolar and bipolar, H Bridge, concept of complementary PWM, generation of sinusoidal PWM Design criteria of inverters. Introduction to multilevel inverters.	6	15%
	INTERNAL TEST 2		
V	Battery Basics, Different types, C- rating, Battery Parameters, packaging, safety, Charging methods, batter standards, Battery modeling, Traction Batteries. Battery testing and monitoring. BMS. Charging schemes, design criteria of battery chargers. SMPS block diagram, Current controlled and voltage controlled schemes and its Applications.	8	20%
VI	Online and off line UPS. Operation of static transfer switch, Solar charge controllers –introduction to MPPT, MPPT algorithms. Active power factor correction (PFC). Surge Protection devices. Magnetic components: Inductors and transformers for high frequency applications. heat sink-Thermal design, types of cooling.	8	20%
	END SEMESTER EXAMINATION		

Course code	Course Name	L-T-P-Credits	Year
07EC7631	**ELECTRONIC PACKAGING AND RELIABILITY**	**3-0-0-3**	**2020**
Pre-requisite(s)	Nil	Total Hours :42	

COURSE OBJECTIVES

The objective of this course is

- To familiarize all the important multidisciplinary area of electronics systems packaging.
- To familiarize the important facets of packaging at three major levels, namely, chip level, board level and system level
- To provide better understanding over the entire spectrum of microelectronic systems packaging from design to fabrication, assembly and testing
- To impart the current trends in packaging of electronic systems

SYLLABUS

Overview of electronic systems packaging, Definition of PWB, Wafer fabrication, inspection and testing, Wafer packaging, Commonly used packages and advanced packages, Electrical Issues, Introduction to DFM, DFR & DFT 20. Components of a CAD package and its highlights, Design Flow considerations, Photo plotting and mask generation, Process flowchart.

COURSE OUTCOME

On completion of the course the student will be able to

1. Understand the basics and advanced concepts of electronic packaging schemes
2. Understand the current trends and special topics of packaging.
3. Understand the Reflow and Wave Soldering methods to attach SMDs

TEXT BOOKS

1. Rao R. Tummala, Fundamentals of Microsystems Packaging, McGraw Hill, NY, 2001

REFERENCES

1. William D.Brown, Advanced Electronic Packaging, IEEE Press, 1999.

NPTEL/ OTHER VIDEO RESOURCES

INTERNAL ASSESSMENT: 40 MARKS

Assessment procedure:

Two internal tests, each having 15%

Tutorials/Assignments/ Mini projects having 10%

End Semester examination having 60%

Module	COURSE PLAN Contents	Contact hours	Semester Exam Marks (%)
I	Overview of electronic systems packaging, Definition of a system and history of semiconductors, Products and levels of packaging, Packaging aspects of handheld products; Case studies in applications, Definition of PWB. Videoon "Sand-to-Silicon", Wafer fabrication, inspection and testing, Wafer packaging; Packaging evolution; Chip connection choices, Wire-bonding, TAB and flipchip-1,Wire bonding, TAB and flipchip-2.	7	15%
II	Necessary of packaging. Types, Single chip packages or modules (SCM),Commonly used packages and advanced packages; Materials in packages, Thermal mismatch in packages; Current trends in packaging, Multi chip modules (MCM)-types; System-in-package (SIP); Packaging roadmaps; Hybrid circuits	5	15%
	INTERNAL TEST 1		
III	Electrical Issues – I; Resistive Parasitic, Electrical Issues – II; Capacitive and Inductive Parasitic, Electrical Issues – III; Layout guidelines and the Reflection problem, Electrical Issues – IV; Interconnection.	5	15%
IV	Benefits from CAD to packages; Introduction to DFM, DFR & DFT 20. Components of a CAD package and its highlights, Design Flow considerations; Beginning a circuit design with schematic work and component layout, Demo and examples of layout and routing; Technology file generation from CAD; DFM check list and design rules; Design for Reliability.	7	15%
	INTERNAL TEST 2		

V	Review of CAD output files for PCB fabrication; Photo plotting and mask generation, Process flow-chart; Vias; PWB substrates, Substrates continued; Video highlights; Surface preparation, Photo-resist and application methods; UV exposure and developing; Printing technologies for PWBs, PWB etching; Resist stripping; Screen-printing technology, Through-hole manufacture process steps; Panel and pattern plating methods. Video highlights on manufacturing; Solder mask for PWBs; Multilayer PWBs; Introduction to micro-vias, Micro-via technology and Sequential build-up technology process flow for high-density interconnects Conventional Vs HDI technologies; Flexible circuits; (Tutorial session)	9	20%
VI	SMD benefits; Design issues; Introduction to soldering, Reflow and Wave Soldering methods to attach SMDs, Solders; Wetting of solders; Flux and its properties; Defects in wave soldering, Vapour phase soldering, BGA soldering and Desoldering/ Repair; SMT failures, SMT failure library and Tin Whiskers, Tin-lead and lead-free solders; Phase diagrams; Thermal profiles for reflow soldering; Lead-free alloys, Lead-free solder considerations; Green electronics; RoHS compliance and e-waste recycling issues. Thermal Design considerations in systems packaging, Introduction to embedded passives; Need for embedded passives; Design Library; Embedded resistor processes Embedded capacitors; Processes for embedding capacitors; Case study.	9	20%
	END SEMESTER EXAMINATION		

Course code	Course Name	L-T-P-Credits	Year
07EC7211	**WIRELESS SENSOR NETWORKS**	**3-0-0-3**	**2020**
Pre-requisite(s)	Wireless Communication	Total Hours :42	

COURSE OBJECTIVES

- To provide knowledge about wireless sensor networks.

SYLLABUS

Wireless Lans, Pans And Mans, Technical issues, network architecture, physical layer, Mac layer, transport layer, middleware protocol group, WLL architecture, technologies, broadband wireless access, Ad-Hoc Wireless Networks, issues-medium access scheme, Wireless Sensor Networks, comparisons with MANET, design challenges, Mac protocols, Energy Management, Security & Reliability, Dynamic power management in sensor networks, unique security challenges in sensor networks and enabling mechanism, security architectures, privacy protection, reliability support in sensor networks, reliability problems in sensor networks, architecture of a distributed sensor system.

COURSE OUTCOME

On completion of the course the student will be able to obtain

1. Thorough knowledge about ad-hoc wireless networks, wireless sensor networks,
2. Better understanding of energy management, security and reliability in wireless Sensor networks.

TEXT BOOKS

1. C. Siva Ram Murthy and B.S Manoj, Ad-hoc wireless networks- architecture and protocols, Pearson education, 2nd, 2005.
2. Mohammad Ilyas and Imag Mahgoub, Handbook of Sensor Networks : Compact Wireless and Wired Sensing Systems, CRC Press 2005.
3. Rajeev Shorey and A.Ananda, Mobile, Wireless and Sensor Networks

REFERENCES

1. Technology, Applications and Future Directions, John Wiley & Sons, 2006.
2. William Stallings, Wireless Communication and Networks, Prentice Hall, 2nd Edition, 2005.
3. Kaveh Pahlavan and Prashant Krishnamurthy, Principle of Wireless Networks- A Unified Approach, Prentice Hall, 2006.

NPTEL/ OTHER VIDEO RESOURCES

INTERNAL ASSESSMENT: 40 MARKS

Assessment procedure:

Two internal tests, each having 15%

Tutorials/Assignments/ Mini projects having 10%

End Semester examination having 60%

Module	COURSE PLAN Contents	Contact hours	Semester Exam Marks (%)
I	Wireless Lans, Pans And Mans: Introduction, fundamentals of WLAN- Technical issues, network architecture, IEEE 802.11- physical layer, Mac layer mechanism, CSMA/CA.	7	15%
II	Bluetooth-specification, transport layer, middleware protocol group, Bluetooth profiles, WLL-generic WLL architecture, technologies, broadband wireless access, IEEE802.16-differences between IEEE 802.11 and 802.16, physical layer, data link layer.	7	15%
	INTERNAL TEST 1		
III	Ad-Hoc Wireless Networks: Introduction, issues medium access scheme, routing, multicasting, transport layer protocol, pricing scheme, QoS provisioning, self-organization, security, addressing, service discovery, energy management, deployment consideration, ad-hoc wireless internet.	7	15%
IV	Wireless Sensor Networks: Introduction applications of sensor networks, comparisons with MANET, issues and design challenges, architecture- layered and clustered, data dissemination, data gathering, Mac protocols, location discovery, quality of sensor networks, coverage in wireless sensor networks- area coverage, point coverage, barrier coverage.	7	15%
	INTERNAL TEST 2		

V	Energy Management, Security & Reliability: Dynamic power management in sensor networks- idle power management, active power management, system implementation, security and privacy protection in wireless sensor networks- unique security challenges in sensor networks and enabling mechanism, security architectures, privacy protection.	7	20%
VI	Reliability support in sensor networks- reliability problems in sensor networks, architecture of a distributed sensor system, distributed services, mechanisms and tools, dynamic adaptation of distributed sensor applications	7	20%
	END SEMESTER EXAMINATION		

Course code	Course Name	L-T-P-Credits	Year
07EC7501	**VLSI SIGNAL PROCESSING**	**3-0-0-3**	**2020**
Pre-requisite(s)	Basic knowledge in signal processing	Total Hours :42	

COURSE OBJECTIVES

- To introduce techniques for altering the existing DSP structures to suit VLSI implementations.
- To introduce efficient design of DSP architectures suitable for VLSI

SYLLABUS

Introduction to DSP systems- Dependence graphs-Loop bound, iteration n bound, Pipelining and Parallel processing for low power, Retiming, unfolding, sample period reduction, Algorithmic strength reduction, Fast convolution algorithms, Pipelined and parallel recursive filters, Bit level arithmetic architectures, CSD representation, CSD multiplication using Horner's rule for precision improvement, Distributed Arithmetic fundamentals and FIR filters, Numerical strength reduction, synchronous pipelining and clocking styles, wave pipelining, Asynchronous pipelining bundled data versus dual rail protocol.

COURSE OUTCOME

On completion of the course the student will have

1. The ability to modify the existing or new DSP architectures suitable for VLSI.

TEXT BOOKS

1. Keshab K. Parhi, " VLSI Digital Signal Processing Systems, Design and implementation ", Wiley, Interscience, 2007.
2. U. Meyer – Baese, " Digital Signal Processing with Field Programmable Gate Arrays", Springer, Second Edition, 2004
3. Allen, J., Computer Architectures for Digital Signal Processing, Proceedings of the IEEE, Vol.73, No.5, May 1985

REFERENCES

1. Bateman A., and Yates, W., Digital Signal Processing Design, Computer Science Press, New York
2. S.Y. Kung, H.J. White House, T. Kailath, VLSI and Modern Signal Processing, Prentice Hall, 1985

NPTEL/ OTHER VIDEO RESOURCES

INTERNAL ASSESSMENT: 40 MARKS

Assessment procedure:

Two internal tests, each having 15%

Tutorials/Assignments/ Mini projects having 10%

End Semester examination having 60%

Module	COURSE PLAN Contents	Contact hours	Semester Exam Marks (%)
I	Introduction to DSP systems – Typical DSP algorithms, Data flow and Dependence graphs - critical path, Loop bound, iteration bound, Longest path matrix algorithm, Pipelining and Parallel processing of FIR filters, Pipelining and Parallel processing for low power.	7	15%
II	Retiming – definitions and properties, Unfolding – an algorithm for unfolding, properties of unfolding, sample period reduction and parallel processing application	7	15%
	INTERNAL TEST 1		
III	Algorithmic strength reduction in filters and transforms – 2-parallel FIR filter, 2-parallel fast FIR filter, DCT architecture, rank order filters, Odd-Even merge-sort architecture, parallel rank-order filters.	7	15%
IV	Fast convolution, Pipelining and parallel Processing of IIR Filters – Cook-Toom algorithm, modified Cook-Toom algorithm, Pipelined and parallel recursive filters – Look-Ahead pipelining in first-order IIR filters, Look-Ahead pipelining with power-of- 2 decomposition, Clustered look-ahead pipelining, Parallel processing of IIR filters, combined pipelining and parallel processing of IIR filters.	7	15%
	INTERNAL TEST 2		

V	Bit-level arithmetic architectures – parallel multipliers with sign extension, parallel carry-ripple and carry-save multipliers, Design of Lyon's bit-serial multipliers using Horner's rule, bit-serial FIR filter, CSD representation, CSD multiplication using Horner's rule for precision improvement, Distributed Arithmetic fundamentals and FIR filters.	7	20%
VI	Numerical strength reduction – sub-expression elimination, multiple constant matching, synchronous pipelining and clocking styles, clock skew in edge-triggered single phase clocking, two-phase clocking, wave pipelining. Asynchronous pipelining bundled data versus dual rail protocol.	7	20%
	END SEMESTER EXAMINATION		

Course code	Course Name	L-T-P-Credits	Year
07EC7603	**CMOS RF CIRCUIT DESIGN**	**3-0-0-3**	**2020**
Pre-requisite(s)	Analog Integrated Circuit Design	Total Hours :42	

COURSE OBJECTIVES

- To impart knowledge on basics of IC design at RF frequencies.

SYLLABUS

Basic Concepts in RF Design, Low-Noise Amplifiers, Mixers, Oscillators, Phase-Locked Loops, Frequency Synthesizers, Power Amplifiers

COURSE OUTCOME

On completion of the course the student will be able to

1. Understand the Basic Concepts in RF Design.
2. Analyze the design of a Low-Noise Amplifiers.
3. Appreciate the different Mixer topologies.
4. Distinguish between different types of Oscillators.
5. Understand various types of Phase-Locked Loops and Frequency Synthesizers.
6. Analyze different Power Amplifiers.

TEXT BOOKS

1. Behzad Razavi, "RF Microelectronics", Prentice Hall.
2. Thomas H. Lee, "The Design of CMOS Radio-Frequency Integrated Circuits", Cambridge University Press.

REFERENCES

1. Abidi, P.R. Gray, and R.G. Meyer, eds., "Integrated Circuits for Wireless Communications", New York: IEEE Press.
2. R. Ludwig and P. Bretchko, "RF Circuit Design, Theory and Applications", Pearson.

NPTEL/ OTHER VIDEO RESOURCES

INTERNAL ASSESSMENT: 40 MARKS

Assessment procedure:

Two internal tests, each having 15%

Tutorials/Assignments/ Mini projects having 10%

End Semester examination having 60%

Module	COURSE PLAN Contents	Contact hours	Semester Exam Marks (%)
I	**Basic Concepts in RF Design:** Effects of Nonlinearity, Noise, Sensitivity and Dynamic Range, Passive Impedance Transformation, Scattering Parameters, Analysis of Nonlinear Dynamic Systems	7	15%
II	**Low-Noise Amplifiers:** Problem of Input Matching, LNA Topologies, Gain Switching, Band Switching, Nonlinearity Calculations.	7	15%
	INTERNAL TEST 1		
III	**Mixers:** Passive Down-conversion Mixers, Active Down-conversion Mixers, Improved Mixer Topologies, Up-conversion Mixers	7	15%
IV	**Oscillators:** Performance Parameters, Basic Principles, Cross-Coupled Oscillator, Three-Point Oscillators, Voltage-Controlled Oscillators, LC VCOs with Wide Tuning Range, Phase Noise, Mathematical Model of VCOs, Quadrature Oscillators.	7	15%
	INTERNAL TEST 2		
V	**Phase-Locked Loops:** Basic Concepts, Type-I PLLs, Type-II PLLs, PFD/CP Non-idealities, Phase Noise in PLLs, Loop Bandwidth, **Integer-N Frequency Synthesizers**: Basic Integer-*N* Synthesizer. **Fractional-N Synthesizers**: Basic Concepts	7	20%
VI	**Power Amplifiers:** General Considerations, Classification of Power Amplifiers, High-Efficiency Power Amplifiers, Cascode Output Stages, Large-Signal Impedance Matching, Basic Linearization Techniques, Polar Modulation, Out-phasing, Doherty Power Amplifier, Design Examples.	7	20%
	END SEMESTER EXAMINATION		

Course code	Course Name	L-T-P-Credits	Year
07EC7613	**DESIGN OF ASIC & SoC**	**3-0-0-3**	**2020**
Pre-requisite(s)	Digital Circuit Design	Total Hours :42	

COURSE OBJECTIVES

- To prepare the student to be an entry-level industrial standard ASIC or FPGA designer.
- To give the student an understanding of issues and tools related to ASIC/FPGA design and implementation.
- To give the student an understanding of basics of System on Chip and Platform based design.
- To demonstrate VLSI tool-flow and FPGA architecture

SYLLABUS

Types of ASICs, Trade off issues at system level, ASIC floor planning, SoC Design, High performance algorithms for ASICs/SoCs

COURSE OUTCOME

On completion of the course the student will be able to

1. Demonstrate VLSI tool-flow and FPGA architecture.
2. Explain the issues involved in ASIC design, including technology choice, design management, tool-flow, verification, debug and test, as well as the impact of technology scaling on ASIC design.
3. Explain the algorithms used for ASIC construction
4. Summarize the basics of System on Chip, On chip communication architectures like AMBA, AXI and utilizing Platform based design.
5. Describe high performance algorithms available for ASICs

TEXT BOOKS

1. M.J.S. Smith, "Application Specific Integrated Circuits", Pearson, 2003
2. S.Pasrich and N.Dutt, "On-Chip Communication Architectures: System on Chip Interconnect", Elsevier, 2008

REFERENCES

1. H.Gerez, "Algorithms for VLSI Design Automation", John Wiley, 1999
2. J..M.Rabaey, A. Chandrakasan, and B. Nikolic, "Digital Integrated Circuit Design Perspective (2/e)", PHI 2003
3. D. A.Hodges, "Analysis and Design of Digital Integrated Circuits (3/e)", MGH 2004
4. Hoi-Jun Yoo, Kangmin Lee and Jun Kyong Kim, "Low-Power SoC for High-Performance SoC Design", CRC Press, 2008

NPTEL/ OTHER VIDEO RESOURCES

INTERNAL ASSESSMENT: 40 MARKS

Assessment procedure:

Two internal tests, each having 15%

Tutorials/Assignments/ Mini projects having 10%

End Semester examination having 60%

Module	COURSE PLAN Contents	Contact hours	Semester Exam Marks (%)
I	Types of ASICs, VLSI Design flow, Programmable ASICs – Anti-fuse, SRAM, EPROM, EEPROM based ASICs. Programmable ASIC logic cells and I/O cells. Programmable interconnects. Latest Version - FPGAs and CPLDs and Soft-core processors.	7	15%
II	Trade off issues at System Level: Optimization with regard to speed, area and power, asynchronous and low power system design. ASIC physical design issues, System Partitioning, Power Dissipation, Partitioning Methods.	7	15%
	INTERNAL TEST 1		
III	ASIC floor planning, Placement and Routing.	7	15%
IV	System-On-Chip Design - SoC Design Flow, Platform-based and IP based SoC Designs	7	15%
	INTERNAL TEST 2		
V	Basic Concepts of Bus-Based Communication Architectures, On-Chip Communication Architecture Standards, Low-Power SoC Design	7	20%
VI	High performance algorithms for ASICs/ SoCs as case studies – Canonic Signed Digit Arithmetic, KCM, Distributed Arithmetic, High performance digital filters for sigma-delta ADC, USB controllers, OMAP.	7	20%
	END SEMESTER EXAMINATION		

Course code	Course Name	L-T-P-Credits	Year
07EC7623	**LOW POWER VLSI**	**3-0-0-3**	**2020**
Pre-requisite(s)	VLSI Design	Total Hours : 42	

COURSE OBJECTIVES

This Course provides insights on

- Various components of power dissipation in CMOS
- Fundamentals of various approaches to low power design
- Low power design techniques.
- To familiarize students with adiabatic circuits

SYLLABUS

Sources of power dissipation, Power estimation, Simulation Power analysis, Low Power Design Circuit level, Low power Clock Distribution

COURSE OUTCOME

On completion of the course the student will be able to

1. Identify sources of power in an IC.
2. Describe the supply voltage scaling approaches
3. Identify various switched capacitance minimization approaches.
4. Explain leakage power minimization approaches
5. Design memory circuits with low power dissipation.
6. Explain adiabatic circuits.

TEXT BOOKS

1. Sung Mo Kang, Yusuf Leblebici, CMOS Digital Integrated Circuits, Tata Mcgraw Hill.
2. Kaushik Roy, Sharat Prasad, "Low-Power CMOS VLSI Circuit Design" Wiley, 2000.
3. Gary K. Yeap, "Practical Low Power Digital VLSI Design", KAP, 2002.
4. Rabaey, Pedram, "Low Power Design Methodologies" Kluwer Academic, 1997.
5. Neil H. E. Weste and K. Eshraghian, Principles of CMOS VLSI Design, 2nd Edition, Addison Wesley (Indian reprint).

REFERENCES

1. "Low – Power Digital VLSI Design, Circuits and Systems", Bellaour& M.I. Elamstry, Kluwer Academic Publishers, 1996.
2. Dimitrios Soudris, Chirstian Pignet, Costas Goutis, "Designing CMOS Circuits for Low Power", Kluwer, 2002.
3. Abdelatif Belaouar, Mohamed.I.Elmasry, "Low power digital VLSI design", Kluwer,1995.
4. "Logic synthesis for Low – power VLSI Designs", B.G.K.Yeap, "Practical Low Power Digital VLSI Design", Kluwer Academic Publishers, 1998.

NPTEL/ OTHER VIDEO RESOURCES

INTERNAL ASSESSMENT: 40 MARKS

Assessment procedure:

Two internal tests, each having 15%

Tutorials/Assignments/ Mini projects having 10%

End Semester examination having 60%

Module	COURSE PLAN Contents	Contact hours	Semester Exam Marks (%)
I	Sources of Power dissipation: Dynamic Power Dissipation, Short Circuit Power, Switching Power, Gliching Power, Static Power Dissipation, Degrees of Freedom	7	15%
II	Supply Voltage Scaling Approaches: Device feature size scaling, Multi-Vdd Circuits, Architectural level approaches: Parallelism, Pipelining, Voltage scaling using high-level transformations, Dynamic voltage scaling, Power Management.	7	15%
	INTERNAL TEST 1		
III	Switched Capacitance Minimization Approaches: Hardware Software Tradeoff Bus Encoding Two's complement Vs Sign Magnitude Architectural optimization Clock Gating Logic styles	7	15%
IV	Leakage Power minimization Approaches: Variable-threshold-voltage CMOS (VTCMOS) approach Multi-threshold-voltage CMOS (MTCMOS) approach Power gating Transistor stacking Dual-V_t assignment approach (DTCMOS)	7	15%
	INTERNAL TEST 2		
V	Design of low power CMOS circuits: Computer arithmetic techniques for low power system – reducing power consumption in memories –low power clock, Inter connect and layout design.	7	20%
VI	Adiabatic circuits-Adiabatic amplification, Adiabatic logic circuits, Pulsed power supply, Partially adiabatic circuits	7	20%
	END SEMESTER EXAMINATION		

Course code	Course Name	L-T-P-Credits	Year
07EC7633	**MEMS and NEMS**	**3-0-0-3**	**2020**
Pre-requisite(s)	Nil	Total Hours: 42	

COURSE OBJECTIVES

- To introduce the students to the concepts of micro electro mechanical systems.
- To enable students to learn the principles MEMS fabrication.
- To impart design principles of micro and Nano-Electro-Mechanical Systems.
- To enable the students to comprehend the theoretical foundations of quantum mechanics and Nano systems

SYLLABUS

Historical Background- Micro-fabrication and Micromachining- Physical Micro-sensors Micro-actuators- Micro-actuator systems-Surface Micromachining- Surface Micro-machined Systems Optical MEMS- Advances in NEMS

COURSE OUTCOME

On completion of the course the student will be able to

1. Understand micro electro mechanical system
2. Classify Physical Micro-sensors.
3. Describe the fabrication processes of surface micromachining.
4. Describe Micro-Opto electro mechanical sensors and systems and its applications.
5. Comprehend the theoretical foundations of quantum mechanics and Nano systems

TEXT BOOKS

1. Stephen D. Senturia, "Microsystem Design" by, Kluwer Academic Publishers, 2001 .
2. Marc Madou, “Fundamentals of Micro fabrication” by, CRC Press, 1997.Gregory.
3. Kovacs, “Micro machined Transducers Sourcebook” WCB McGraw-Hill, Boston

REFERENCES

1. M.-H. Bao, “Micromechanical Transducers: Pressure sensors, accelrometers, and gyroscopes” by Elsevier, New York, 2000.
2. Gabriel M. Rebeiz, RF MEMS, Theory, Design, and Technology, Wiley Interscience.
3. Sergey Edward Lyshevski, —MEMS and NEMS: Systems, Devices, and Structures‖ CRC Press, 2002

NPTEL/ OTHER VIDEO RESOURCES

INTERNAL ASSESSMENT: 40 MARKS

Assessment procedure:

Two internal tests, each having 15%

Tutorials/Assignments/ Mini projects having 10%

End Semester examination having 60%

Module	COURSE PLAN Contents	Contact hours	Semester Exam Marks (%)
I	Historical Background, Silicon Pressure sensors, Micromachining, Micro Electro Mechanical Systems. Micro-fabrication and Micromachining: Integrated Circuit Processes, Bulk Micromachining: Isotropic Etching and Anisotropic Etching, Wafer Bonding, High Aspect-Ratio Processes (LIGA).	7	15%
II	**Physical Micro-sensors :** Classification of physical sensors, Integrated, Intelligent, or Smart sensors, Sensor Principles and Examples : Thermal sensors, Electrical Sensors, Mechanical Sensors, Chemical and Biosensors	7	15%
	INTERNAL TEST 1		
III	**Micro-actuators:** Electromagnetic and Thermal micro-actuation, Mechanical design of micro-actuators, Micro-actuator examples, micro-valves, micro-pumps, micro-motors-Micro-actuator systems : Success Stories, InkJet printer heads, Micro-mirror TV Projector.	7	15%
IV	**Surface Micromachining:** One or two sacrificial layer processes, Surface micro-machining requirements, Polysilicon surface micromachining, Other compatible materials, Silicon Dioxide, Silicon Nitride, Piezoelectric materials, Surface Micro-machined Systems: Success Stories, Micro-motors, Gear trains, Mechanisms.	7	15%
	INTERNAL TEST 2		
V	**Optical MEMS:** Micro opto electro mechanical sensors and systems, fiber optic sensors, Fiber Bragg grating, miniature sensors for temperature, pressure, fluid flow applications.	7	20%
VI	Atomic Structures and Quantum Mechanics, Shrodinger Equation, ZnO Nano-rods based NEMS device: Gas sensor.	7	20%

Course code	Course Name	L-T-P-Credits	Year
07EC7643	**EMBEDDED NETWORK PROTOCOLS**	**3-0-0-3**	**2020**
Pre-requisite(s)	Nil	Total Hours :42	

COURSE OBJECTIVES

- Introduce buses used in embedded systems
- Introduce industrial grade communication interfaces used in embedded systems
- Familiarize connectivity between various embedded systems and PC
- Connectivity to internet via wired and wireless communication channels

SYLLABUS

Introduction to Embedded Networking, Serial Communication Protocols, PC Parallel port programming, USB Bus, USB Bus Communication, Microcontroller USB interface, CAN Bus, PIC Microcontroller CAN interface, Micro CAN, Elements of a Network, Design Choices, Inside the internet protocol, Wireless Embedded Networking

COURSE OUTCOME

On completion of the course the student will be able to

1. Implement different communication channels and its protocols with signaling inside the embedded systems and to the outside world.
2. Explain the serial and parallel communication strategies used in Embedded Systems
3. Explain the working of SPI and I2C networking protocols
4. Explain the role of USB in peripheral communication Interpreting the format and role of CAN protocol in Automobile communications
5. Associate different wired and wireless networking protocols used in device communication

TEXT BOOKS

1. Wayne Wolf, "Computers as Components: Principles of Embedded Computing System Design", Morgan Kaufman Publishers, 2008.
2. Olaf P Feiffer, Andrew Ayre & Christian Keyold, "Embedded Networking with CAN and CAN Open", Embedded System Academy, 2005
3. Marco Di Natale, Haibo Zeng, Paolo Giusto &Arakadeb Ghosal, "Understanding and Using the Controller Area Network", Springer, 2012
4. Lyla B Das, "Embedded Systems-An Integrated Approach", Pearson, 2012.
5. Dr. SidnieFeit, "TCP/IP : Architectures, Protocols and Implementations with IPv6 and IP Security", Tata McGraw Hill, Second Edition, 2008

REFERENCES

1. NXP Semiconductors, "I2C-bus Specification and User Manual", Rev. 5, October 2012. (Available at http://www.nxp.com/documents/user_manual/UM10204.pdf)
2. https://www.cypress.com/file/134171/download
3. Motorola Inc., "S12SPIV3/D: SPI Block Guide V03.06", Feb 2003, (Available at http://www.ee.nmt.edu/~teare/ee308l/datasheets/S12SPIV3.pdf).

NPTEL/ OTHER VIDEO RESOURCES

INTERNAL ASSESSMENT: 40 MARKS

Assessment procedure:

Two internal tests, each having 15%

Tutorials/Assignments/ Mini projects having 10%

End Semester examination having 60%

Module	COURSE PLAN Contents	Contact hours	Semester Exam Marks (%)
I	Introduction to Embedded Networking, Serial/Parallel Communication – Serial communication protocols -RS232 standard – RS485 – Firewire (IEEE 1394). Synchronous Serial Protocols -Serial Peripheral Interface (SPI) – Inter Integrated Circuits (I2C) – PC Parallel port programming - ISA/PCI Bus protocols	7	15%
II	SPI : Introduction, Features, Modes of Operation, External Signal Description, Functional Description(Covering Master Mode, Slave Mode, Transmission Formats, Baud Rate Generation, Error Conditions, Low Power Mode Options) I2C : I2C-bus features, Modes of Operation -Standard-mode, Fast-mode, Fast-mode plus, Ultra fast mode(covering the following topics - Signals and Logic levels, Start/Stop conditions, byte format, Acknowledge and Not-Acknowledge, Clock Synchronization, Arbitration, Clock Stretching, Addressing, Call Addresses, Reset, Device ID), Applications of I2C bus protocol.	7	15%
	INTERNAL TEST 1		
III	USB bus – Introduction – Speed Identification on the bus – USB States, USB bus communication: Packets –Data flow types –Enumeration –Descriptors –USB OTG, USB device, PIC 18 Microcontroller USB Interface. Introduction to USB 3.0	7	15%

IV	Controller Area Network: CAN Overview, Introduction, CAN 2.0b Standard (covering Physical Layer, Message Frame Formats, Bus Arbitration, Message Reception and Filtering, Error Management), CAN Controllers, CAN Development Tools.	7	15%
	INTERNAL TEST 2		
V	TCP/IP: TCP/IP: Introduction to TCP/IP: History, Architecture, Standards and Applications, TCP/IP Architecture: Layering, Protocol Overview, Routers & Topology, IP routing, TCP Architecture, UDP Architecture, Security Concepts.	7	20%
VI	ZigBee: Introduction, Comparison with Bluetooth, Short range wireless networking classes, Zigbee & IEEE802.15.4 standard, Operating frequencies, data rate, interoperability, Device types, Topologies, Communication basics, Association and Disassociation, binding, Self-forming and self-healing characteristics, Networking Layer functions, ZigBee gateway, Zigbee Metaphor, Networking Examples - Home Automation	7	20%
	END SEMESTER EXAMINATION		

Course code	Course Name	L-T-P-Credits	Year
07EC7653	**RTOS FOR MULTI-CORE ENVIRONMENT**	**3-0-0-3**	**2020**
Pre-requisite(s)	Nil	Total Hours :42	

COURSE OBJECTIVES

- To familiarize the student on Real-time Operating Systems and its role in Multi Core Processor environments

SYLLABUS

Introduction to Real-time Systems – Functions of RTOS Kernel – Tasks – Task Scheduling Algorithms – Inter-task communication and synchronization - Deadlocks – Priority inversion – Multi Tasking and Multi Core architectures – Challenges – Instruction Level Parallelism – Thread level parallelism – Mutex, semaphore and message queues – Scheduler and multi-core scheduling – Multi Core SoC – Parallelism –Multiprocessing – Symmetric Multiprocessing – Asymmetric Multiprocessing

COURSE OUTCOME

On completion of the course the student will be able to

1. Explain the fundamental concepts of Real-time systems
2. Identify the various components needed to implement an RTOS
3. Exemplify the issues related to Multi core and Multiprocessor architectures
4. Explain the techniques used to address the challenges of a multitasking environment

TEXT BOOKS

1. Philip A. Laplante, "Real-time System Design and Analysis," Third Edition, PHI, 2004.
2. Jane W.S. Liu, "Real–Time Systems", First Edition, Pearson Education, 2000.
3. Kevin Roebuck, "AUTOSAR – Automotive Open System Architecture: High–Impact Strategies – What You Need to Know: Definitions, Adoptions, Impact, Benefits, Maturity, Vendors", Emereo Pty Limited, 2011.
4. J.L. Hennessy and D.A. Patterson, "Computer Architecture: A Quantitative Approach", Fifth Edition, Morgan Kaufmann, 2011.

REFERENCES

1. Georgios Kornaros, "Multi–core Embedded Systems", First Edition, CRC Press, 2010.
2. William Stallings, Operating systems: Internals and Design Principles, Eighth edition, Prentice Hall.2012

NPTEL/ OTHER VIDEO RESOURCES

INTERNAL ASSESSMENT: 40 MARKS

Assessment procedure:

Two internal tests, each having 15%

Tutorials/Assignments/ Mini projects having 10%

End Semester examination having 60%

Module	COURSE PLAN Contents	Contact hours	Semester Exam Marks (%)
I	Real-time operating systems (RTOS) basics: Introduction to Real-time systems –characteristics, features and types, operating system basics, services, kernel architecture, functions of RTOS kernel, existing RTOS category, Tasks, Process and Threads,	7	15%
II	Task classification, task states, state transitions, task control block, task management, task scheduling– fixed priority and dynamic priority scheduling algorithms. Inter–task communication and synchronization, semaphores–inheritance, inversion, ceiling, deadlocks and starvation, priority inversion and mutexes, how to choose a RTOS for an application.	7	15%
	INTERNAL TEST 1		
III	Multi-tasking and Multi-core architectures: The challenges of multitasking and real-time, achieving multitasking with sequential programming, Instruction level parallelism (ILP), Static & Dynamic scheduling, Thread level parallelism, Multi–issue and Multi–core processors	7	15%

IV	Shared and Distributed memory Multiprocessor Architectures – mutex, semaphore and message queues, Multi–core architectures for embedded systems, Memory issues in multi-core software, working with cache memory, memory contention, false sharing, memory consistency and inconsistency. Scheduler and multi-core scheduling, multiprocessing and multitasking.	7	15%
	INTERNAL TEST 2		
V	Multi-core Systems-on-a-Chip: Amdahl's law, Fine-grained Vs Coarse-grained parallelism, Symmetric Vs Asymmetric Multiprocessing, operating systems for embedded multiprocessing,	7	20%
VI	Symmetric Multiprocessing (SMP): operating systems support for SMP, Spinlocks, load balancing Vs Processor affinity, OpenMP. Asymmetric Multiprocessing (AMP): when to use AMP, operating systems for AMP, moving from uni-processing to AMP. RTOS for multi-core systems.	7	20%
	END SEMESTER EXAMINATION		

Course code	Course Name	L-T-P-Credits	Year
07EC7605	**SEMINAR - II**	**0-0-2-2**	**2020**
Pre-requisite(s)	Nil	Total Hours :	

COURSE OBJECTIVES

This course is intended for

- Increasing the breadth of knowledge
- Enhancing the ability of self-study
- Improving presentation and communication skills
- Augmenting the skill of Technical Report Writing.

OUTLINE AND EVALUATION PROCEDURE

Students have to register for the seminar and select a topic in consultation with any faculty member offering courses for the programme. A detailed write-up on the topic of the seminar is to be prepared in the prescribed format given by the Department. The seminar shall be of 30 minutes duration and a committee with the Head of the department as the chairman and two faculty members from the department as members shall evaluate the seminar based on the report and coverage of the topic, presentation and ability to answer the questions put forward by the committee. Faculty member in charge of the seminar and another faculty member in the department nominated by the Head of the Department are the evaluators for the seminar.

Internal Assessment: 100 Marks

The distribution of marks for seminar is as follows

Marks for the report: 30%

Presentation: 40%

Ability to answer questions on the topic: 30%

COURSE OUTCOME

1. Debating capability and presentation skills in a technical topic of his interest.
2. Knowledge about contemporary issues and research opportunities
3. Capacity to communicate effectively and professionally in both verbal and written forms
4. Capability for self-education and lifelong learning.

Course code	Course Name	L-T-P-Credits	Year
07EC7607	**PROJECT(Phase-I)**	**0-0-12-6**	**2020**
Pre-requisite(s)	Nil	Total Hours :--	

COURSE OBJECTIVES

- To identify current issues in the area of VLSI and Embedded systems
- To improve the professional competency and research aptitude by touching the areas which otherwise not covered by theory or laboratory classes.
- The project work aims to develop the work practice in students to apply theoretical and practical tools/techniques to solve real life problems related to industry and current research.

OUTLINE AND EVALUATION PROCEDURE

The student is required to undertake the project phase-I during the third semester and is continued in the 4th semester (Phase-II). Normally students are expected to do the project within the college. However they are permitted to do the project in an Industry or in a government research institute under a qualified supervisor from that organization. Progress of the project work is to be evaluated at the end of the third semester. For this a committee headed by the head of the department with two other faculty members in the area of the project and the project supervisor/s. If the project is done outside the college, the external supervisor associated with the student shall also be a member of the committee. Phase-I consists of preliminary thesis work, two reviews of the work and the submission of preliminary report. First review should highlight the topic, objectives, methodology and expected results. Second review assesses the progress of the work, preliminary report and future plan of the work to be completed in the 4th semester. A preliminary report consisting of the work completed and scope of the work for the 4th semester should be submitted to the Head of department.

Project Progress evaluation details: Marks:50

Progress evaluation by the Project Supervisor: 20 Marks

Presentation and evaluation by the committee: 30 Marks

COURSE OUTCOME

1. Knowledge about contemporary issues and research opportunities
2. Capacity to communicate effectively and professionally in both verbal and written forms
3. Capability of self-education and lifelong learning
4. Understanding of professional and ethical responsibility

SEMESTER -4
SYLLABI

Course code	Course Name	L-T-P-Credits	Year
07EC7602	**PROJECT (Phase-II)**	**0-0-21-12**	**2020**
Pre-requisite(s)	Nil	Total Hours :--	

COURSE OBJECTIVES

- To improve the professional competency and research aptitude by touching the areas which otherwise not covered by theory or laboratory classes.
- The project work aims to develop the work practice in students to apply theoretical and practical tools/techniques to solve real life problems related to industry and current research.

OUTLINE AND EVALUATION PROCEDURE

Project phase-II is a continuation of project phase-I started in the third semester. There would be two reviews in the 4th semester, first in the middle of the semester and the second at the end of the semester. First review is to evaluate the progress of the work. Second review would be a pre-submission presentation before the evaluation committee to assess the quality and quantum of the work done. This would be a pre-qualifying exercise for the students for getting approval by the Departmental committee for the submission of the thesis. Final evaluation of the project will be taken up only if the student has earned all course credits listed in the first three semesters. Project evaluation shall be done by the same committee constituted in the third semester with an external expert, either from an academic/R&D organization or from Industry, as an additional member. Final project grading shall take into account the progress evaluation done in the third semester and the project evaluation in the fourth semester. If the quantum of work done by the candidate is found to be unsatisfactory, the committee may extend the duration of the project up to one more semester, giving reasons for this in writing to the student. Normally further extension will not be granted and there shall be no provision to register again for the project. At least one technical paper is to be prepared for possible publication in journal or conferences. The technical paper is to be submitted along with the thesis. The final evaluation of the project will be external evaluation.

Project Progress evaluation details: Marks:100

Project evaluation by the supervisor/s : 30 Marks

Presentation & evaluation by the Committee : 40 Marks

Evaluation by the External expert : 30 Marks

COURSE OUTCOME
The graduate will have acquired 1. Knowledge about contemporary issues and research opportunities 2. Capacity to communicate effectively and professionally in both verbal and written forms 3. Capability of self-education and lifelong learning 4. Understanding of professional and ethical responsibility

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