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APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

FIFTH SEMESTER B. TECH (HONOURS) DEGREE EXAMINATION, DECEMBER 2017

Course Code: EE365

Course Name: DIGITAL SYSTEM DESIGN (EE)

Max. Marks: 100 Duration: 3 Hours

PART A

Answer all questions, each carries 5 marks.

		Marks
1	Implement a Full Adder circuit using NAND gates alone. Also write the truth table.	(5)
2	For the below VHDL code, assume that the values of A, B, C and D are all integers with value 0 at time = 10ns. If E changes from 0 to 2 at time = 20ns. Specify the time at which each signal will change and value to which it will change. List the changes in chronological order (20ns, 20+Δ ns, 20+2Δ ns.)	(5)

```
p1: process
begin
        wait on E;
        A <= 1 after 5ns;
        B <= A+1;
        C <= B after 10ns;
        wait for 0ns;
        D <= B after 3ns;
        A <= A+5 after 15ns;
        B <= B+7;
end process p1;
```

3	Explain Mealy and Moore state diagram with the help of a block diagram.	(5)
4	Model an edge triggered d flip-flop using VHDL program.	(5)
5	What is meant by event driven simulation? Explain with the help of example.	(5)
6	What is the need of fault modelling in integrated circuits? Explain different fault models.	(5)
7	What is meant by Fault oriented Test Pattern Generation? Explain the general fault-oriented test generation strategy adopted in order to generate a minimum number of test patterns,	(5)
8	What are undetectable faults? Explain with the help of example.	

PART B

Answer any two full questions, each carries 10 marks.

9	a)	Explain inertial delay and transport with an example VHDL modelling.	(3)
	b)	Write a VHDL test-bench to validate two input AND gate.	(4)
	c)	Explain the difference between a signal assignment and variable assignment with example.	(3)
10	a)	What is the function of a multiplexer? Implement a 4 to 1 multiplexer using AOI logic (AND, OR, NOT gates). Write the truth table.	(4)
	b)	Write the VHDL code to model a 4 to 1 multiplexer.	(6)
11	a)	Explain the different number codes used in digital systems. State the purpose of using Parity bits.	(5)
	b)	Model a Parity checker using VHDL program.	(5)

PART C

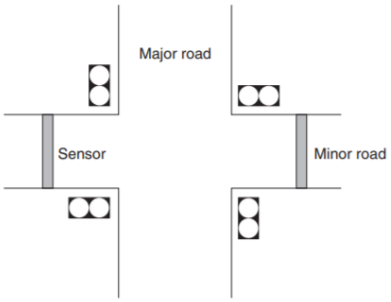
Answer any two full questions, each carries 10 marks.

12 a) Explain sensitivity list (3)

b) Draw a truth table for J-K flops with synchronous active low set and preset. (3)

c) Write a VHDL code for the above mentioned model of a J-K flop (4)

13 Design, using an ASM chart, a traffic signal controller for a crossroads. The traffic signals have two lights each – red and green. The major road normally has a green light, while the minor road has a red light. If a car is detected on the minor road, the signals change to red for the major road and green for the minor road. When the lights change, a timer is started. Once that timer completes, a 'TIMED' signal is asserted, which causes the lights to change back to their default state. Design an implementation that uses a minimal number of D flip-flops. Consider only straight signal (no left signal and right signal). (10)



14 Write a VHDL description for a self-correcting Johnson counter which corrects itself when the counter goes into parasitic sequence. Given below is the normal sequence and parasitic sequence. (10)

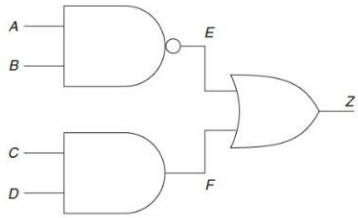
Normal counting sequence	Parasitic counting sequence
0000	0010
1000	1001
1100	0100
1110	1010
1111	1101
0111	0110
0011	1011
0001	0101

PART D

Answer any two full questions, each carries 10 marks.

15 With the help of examples, explain the constraints in RTL synthesis. (10)

16 Considering the given circuit as model, explain how sensitive path algorithm can be used to detect faults. (Make necessary assumptions). (10)



17 a) Explain the different VHDL simulation modelling issues. (5)

b) Explain the difference between parallel and concurrent fault simulation. (5)

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