

Reg No.: \_\_\_\_\_

Name: \_\_\_\_\_

**APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY**  
**FIRST SEMESTER MCA DEGREE EXAMINATION, DECEMBER 2017**

**Course Code: RLMCA109**

**Course Name: DIGITAL FUNDAMENTALS**

Max. Marks: 60

Duration: 3 Hours

**PART A**

*Answer all questions, each carries 3 marks.*

Marks

- |   |   |     |
|---|---|-----|
| 1 | Convert $3.248 \times 10^4$ into single precision floating point binary number. | (3) |
| 2 | Justify the statement: NAND and NOR gates are universal gates                   | (3) |
| 3 | Specify the minterms of $A+BC$ .  | (3) |
| 4 | Compare and contrast ripple carry adder and carry look ahead adder.             | (3) |
| 5 | What is a de-multiplexer?   | (3) |
| 6 | Differentiate between combinational logic and sequential logic circuits.        | (3) |
| 7 | Why asynchronous counters are also known as ripple counters?                    | (3) |
| 8 | What do you mean by a Modulo-N Counter?   | (3) |

**PART B**

*Answer six questions, one full question from each module and carries 6 marks.*

**Module I**

- |   |  |     |
|---|--|-----|
| 9 | a) Convert 1110001.0001 to decimal and hexadecimal.                              | (3) |
|   | b) Given $A = 1001010$ and $B = 1000$ . Perform $A-B$ , $A/B$ and $A \times B$ . | (3) |

**OR**

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|----|--|-----|
| 10 | a) Convert the pair into binary and add using 2's complement: -72 and 27.      | (3) |
|    | b) Express -34 in sign magnitude, 1's complement form and 2's complement form. | (3) |

**Module II**

- |    |  |     |
|----|--|-----|
| 11 | a) State and prove (i) $A+A'B=A+B$ , (ii) $A+AB=A$ . | (3) |
|    | b) State and prove Demorgan's Theorems.              | (3) |

**OR**

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|----|--|-----|
| 12 | Simplify using K-Map $y = \sum (0,1,3,5,9,12) + \sum d(2,4,6,7)$ | (6) |
|----|--|-----|

**Module III**

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|----|--|-----|
| 13 | Implement the Boolean function $F(A, B, C, D) = \sum (1,3,4,11,12,13,14,15)$ using 8-to-1 multiplexer. | (6) |
|----|--|-----|

**OR**

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|----|---|-----|
| 14 | Explain the working principle of full adder in detail. Design a full adder using a decoder. | (6) |
|----|---|-----|

**Module IV**

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|----|---|-----|
| 15 | J K flip-flop can be used for solving the 'indeterminate state' in SR Flip-flop. Justify the statement. | (6) |
|----|---|-----|

**OR**

- 16 What is the disadvantage of level triggering? How can we overcome it by using master slave Flip-flop? (6)

**Module V**

- 17 Classify shift registers based on the data movement in register. (6)

**OR**

- 18 Differentiate between up asynchronous counter and down asynchronous counter with suitable logic diagrams. (6)

**Module VI**

- 19 Describe the components of a computer with a block diagram. (6)

**OR**

- 20 Explain in detail about the hardware and software components of an Arduino board. (6)

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