Reg. No._____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

SECOND SEMESTER MCA DEGREE EXAMINATION, APRIL 2018

Course Code: RLMCA112

Course Name: COMPUTER ORGANIZATION AND ARCHITECTURE

Max Marks: 60 Duration: 3 Hours

PART A

Answer all questions. Each question carries 3 marks.

1. What is System Software? Write any two examples of System software.
2. Distinguish between memory mapped I/O and I/O mapped I/O.
3. Explain multiple bus organization with a neat diagram.
4. Write the sequence of control steps required for the instruction: ADD R1, R2,R3 in a three bus architecture.
5. Discuss any two methods for handling interrupts from multiple devices.
6. Differentiate between SRAM and DRAM cells.
7. Construct a 4M X 16 memory module using 256K X 4 memory chips.
8. What is Cache hit and Cache miss? Discuss Cache Coherence problem.

PART B

Answer any one question from each module. Each question carries 6 marks.

MODULE I

9. a. What is a system bus? Discuss various bus structures. (3)
   b. Discuss any two bus arbitration methods. (3)

OR

10. What are Branch Instructions? Discuss the execution sequence of Branching instructions (Jump and Conditional Branching) with the help of examples.

MODULE II

11. Explain how data transfer takes place between processor and I/O device in Program Controlled I/O technique with an example.

OR

12. Discuss subroutine linkage method. And explain how nested subroutines are implemented.

MODULE III

13. Discuss the organization of hardwired Control Unit.

OR

14. Draw and explain the block diagram of typical Microprogrammed Control Unit

MODULE IV

15. What is DMA? Explain its operation.

OR

16. Discuss the working of USB.

MODULE V

17. Explain the working of a DRAM and SDRAM with block diagrams

OR

18. Explain the internal organization of a dynamic memory chip and design 1K* 8 memory chip using decoders.

MODULE VI

19. What is Segmentation? Explain the segmentation hardware with a neat diagram.

OR

20. Discuss any two different types of cache mapping schemes. A set-associate cache consists of a total of 64 blocks divided into four-block sets. The main memory contains 4096 blocks, each consisting of 128 words. How many bits are there in the main memory address? How many bits are there in each of the TAG, SET and WORD fields?