

Name :  
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APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY  
07 THRISSUR CLUSTER

SECOND SEMESTER M.TECH. DEGREE EXAMINATION APRIL 2018

Department of Electronics and communication Engineering

Communication Engineering and Signal Processing

07EC6206 Real Time Digital Signal Processing

Time : 3 hours

Max.Marks: 60

Answer all six questions. Part 'a' of each question is compulsory.

Answer either part 'b' or part 'c' of each question

| Q.no. | Module 1  | Marks |
|-------|---|-------|
| 1a    | Write short note on MCBSP with suitable sketch.   | 4     |
|       | <b>Answer b or c</b>  |       |
| b     | Explain how interrupts effects the working of a DSP unit.   | 5     |
| c     | Differentiate between TMS320C6713 and TMS320C6416 DSP processors.   | 5     |
| Q.no. | Module 2  | Marks |
| 2a    | Discuss on different types of instruction set in a DSP processor.   | 4     |
|       | <b>Answer b or c</b>  |       |
| b     | Explain about the register sets of TMS320C6713 and how these registers are involved in accessing memory unit. | 5     |
| c     | Write an assembly source program to detect a stored four digit code.  | 5     |
| Q.no. | Module 3  | Marks |
| 3a    | Write the matlab code to find the DFT of any given sequence.  | 4     |
|       | <b>Answer b or c</b>  |       |
| b     | Write short note on code composer studio and the different types of file types used in it.                    | 5     |
| c     | Compute DIT- DFT for the sequence $x(n) = \{1,2,3,4,4,3,2,1\}$  | 5     |
| Q.no. | Module 4  | Marks |
| 4a    | Obtain the parallel form realization for the transfer function  | 4     |

$$H(z) = (1 + 3z^{-1} + 2z^{-2}) / (1 + \frac{3}{8}z^{-1} - \frac{3}{32}z^{-2} - \frac{1}{64}z^{-3})$$

**Answer b or c**

- |          |   |          |
|----------|---|----------|
| <b>b</b> | Explain how a DTMF tone is generated, detected and displayed. | <b>5</b> |
| <b>c</b> | Explain in detail about VHDL architecture.                    | <b>5</b> |

| Q.no. | Module 5  | Marks |
|-------|---|-------|
| 5a    | Write short note on data objects and identifiers of VHDL. | 5     |

**Answer b or c**

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|----------|--|----------|
| <b>b</b> | Explain in detail about the architecture of FPGA     | <b>7</b> |
| <b>c</b> | Explain the need of state minimization with example. | <b>7</b> |

| Q.no. | Module 6  | Marks |
|-------|---|-------|
| 6a    | Explain in detail about distributed algorithm method. | 5     |

**Answer b or c**

- |          |   |          |
|----------|---|----------|
| <b>b</b> | Discuss on block processing, pipelining and folding concepts involved in the design of a DSP circuit. | <b>7</b> |
| <b>c</b> | Derive an algorithm for finding the FFT of any given sequences.                                       | <b>7</b> |