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APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

07 THRISSUR CLUSTER

SECOND SEMESTER M.TECH. DEGREE EXAMINATION APRIL 2017

Electronics & Communication Engineering

(Embedded Systems)

07EC6402 DESIGN OF DIGITAL SIGNAL PROCESSING SYSTEMS

Time:3 hours **Max.marks: 60**

Answer all six questions. Part 'a' of each question is compulsory.

Answer either part 'b' or part 'c' of each question

Q.no.	Module 1	Marks
1a	With necessary diagrams explain the CPU architecture of TMS320C67XX devices?	**4**
	Answer b or c	
b	Write short note on interrupt signals of TMS320C6XXX processors?	**5**
c	Write short note on CPU Data-path Control of TMS320C6XXX processors?	**5**

Q.no.	Module 2	Marks
2a	Write short notes on pipeline operation in the following instruction types: i) Single Cycle Instructions ii) 4 Cycle Instructions iii) ADDDP Instructions iv) MPYSP2DP Instructions	**4**
	Answer b or c	
b	Write short note about internal data/program cache of TMS320C6XXX series?	**5**
c	Explain about External Memory Interfacing in TMS3206713 DSP processors?	**5**

Q.no.	Module 3	Marks
3a	i) What will be the value of registers after execution of the following instructions; a) CMPGT .L1 8,A1,A2; A1 = 00000023H b) SHR .S2 B0,B1,B2; B0 = F4925555H and B1 = 00000012H ii) Draw the fetch packet structure & pipeline operation flow of the given program segment; instruction A instruction B || instruction C instruction D || instruction E || instruction F instruction G instruction H	4
	Answer b or c	
b	Write a C program that calls an assembly function that calculates the following equation: [a2 + (a+1)2+ (a+2)2] - [b2 + (b+1)2 + (b+2)2], where a = 3 and b = 2?	5
c	Explain in details on any two instruction set types supported by TMS320C67XX processors?	5

Q.no.	Module 4	Marks
4a	Explain the following filter design functions; 1) [b,a] = butter (4, 0.4); 2) [b,a] = cheby1(5,1,[0.4 0.7]); 3) [b,a] = cheby2(6,80,0.8,'high'); 4) [b,a] = ellip(37,1,40,[0.4 0.7],'stop');	4
	Answer b or c	
b	Determine the DFT and IDFT of the given sequence x[n] = {1,3,4} and prove that IDFT is the inverse of DFT?	5
c	Determine X(k) of the given sequence x[n] = {0,1,2,4,6,5,3,7} using DIT FFT algorithm?	5

Q.no.	Module 5	Marks
5a	With necessary diagrams (if any) explain the real-time implementation methodology of FIR filters on DSP processors?	5
	Answer b or c	
b	Write the program for implementing a real time high-pass FIR filter on TMS320C6713 processor if the filter co-efficients are given as;	7

Float tri1[31]={0.000000, -0.001185, -0.003336, -0.005868, -0.007885, -0.008298,-0.005988, 0.000000, 0.010265, 0.024895, 0.043368, 0.064545, 0.086737, 0.107877, 0.125747, 0.138255, 0.125747, 0.107877, 0.086737, 0.064545, 0.043368, 0.024895, 0.010265, 0.000000, -0.005988, -0.008298, -0.007885, -0.005868, -0.003336,-0.001185, 0.000000};

c	With necessary diagrams explain the conceptual idea of DTMF tone detection implementation?	**7**

Q.no.	**Module 6**	**Marks**
6a	Determine the convolution sum of the given sequences using Distributed Arithmetic and also prove the numerical validity of the result obtained? x[n] = {1,2,8,14} and c[n] = {1,3,2,5}	**5**
	Answer b or c	
b	Explain the Cooley Tukey FFT algorithm implementation in FPGA based DSP controllers?	**7**
c	Write short note on modified DA architecture used in FPGA DSP Technology?	**7**