Name :
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APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

07 THRISSUR CLUSTER

SECOND SEMESTER M.TECH. DEGREE EXAMINATION APRIL 2018

Department of Electronics and communication Engineering

Communication Engineering and Signal Processing

07EC6206 Real Time Digital Signal Processing

Time : 3 hours **Max.Marks: 60**

Answer all six questions. Part 'a' of each question is compulsory.

Answer either part 'b' or part 'c' of each question

Q.no.	Module 1	Marks
1a	Write short note on external memory interface of TMS320C6X DSP processor.	**4**
	Answer b or c	
b	With neat sketch explain the architecture of TMS320C6713 processor.	**5**
c	Discuss about the data path and controlling units of DSP processor.	**5**

Q.no.	Module 2	Marks
2a	Write down the assembly code to find the sum of n+(n-1)+(n-2)+……1	**4**
	Answer b or c	
b	Explain the instruction set and addressing modes of DSP processor.	**5**
c	Write down the assembly code to multiply datas stored in two arrays.	**5**

Q.no.	Module 3	Marks
3a	Write down the matlab code for finding the frequency response of a chebyshev HPF.	**4**
	Answer b or c	
b	Derive the expression for designing FIR filter using window method and discuss on the need of using window function.	**5**
c	Design an ideal HPF filter with frequency response.	**5**

$$H_d(e^{j\omega}) = \begin{cases} 1 \quad for \ \frac{\pi}{4} \leq \ |\omega| \ \leq \pi \\ 0 \ for \ |\omega| \leq \frac{\pi}{4} \end{cases}$$

For N=11 using hamming window'

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Q.no.	Module 4	Marks
4a	Explain about entities and architecture in VHDL.	**4**
	Answer b or c	
b	Explain how a DTMF tone is generated and detected using Goertzel algorithm.	**5**
c	Derive the radix 4 FFT algorithm for finding DFT of any given sequence.	**5**

Q.no.	Module 5	Marks
5a	Discuss on the VHDL delay models.	**5**
	Answer b or c	
b	Design an FSM that has an input *w* and output *z*. The machine is a sequence detector that produces z=1 when previous two values of *w* were 00 or 11; else *z*=0.	**7**
c	Design a MOD 8 counter with VHDL coding.	**7**

Q.no.	Module 6	Marks
6a	Write short note on retiming and pipelining concepts involved in the design of a DSP circuit.	**5**
	Answer b or c	
b	Explain about various performance measures involved a VLSI circuit.	**7**
c	Explain SOC architecture.	**7**