DEPARTMENT OF TECHNICAL EDUCATION <u>GOVERNMENT ENGINEERING COLLEGE</u>, THRISSUR

No.D1/1958 /2016

Dated: 26 /5/17

SHORT TENDER NOTICE

Sealed Tenders are invited for the supply of Equipments/Consumables for Govt. Enginering college, Thrissur.

SI. No	Tender No.	Name of lab	Items & Specification	Last date of issue	Last date of reciept	Date of opening	Tender value	App.Cost
1	D1/34/ 17-18	Civil Engineering	Data Acquisition System	29/6/17 12Noon	29/6/17 2 PM	30/6/17 11 AM	1418/- + Postal Charges	4,50,000/-
2	D1/35/ 17-18	Electrical Engineering	NI DAQ PCleAQ PCle6353 Control Board and related accessories	29/6/17 12Noon	29/6/17 2 PM	306/17 11 AM	1418/- + Postal Charges	4,89 ,000/-

Total AS = Rs.932,000 /-

Phone No.0487-2334144

Website. www.gectcr.ac.in

Intending tenderers may obtain the requisite tender form from Principal, Govt. Engineerig College, Thrissur on cash remittance of cost of Tender form + postal charge. Tender forms are not transferable. Late Tenders will not be accepted. Application for the tender form should be accompanied by cash remittance, as per the price fixed for the tender form.

Cheques, Postages stamps etc will not be accepted towards the cost of the forms nor the forms will be sent by VPP.

Tenders should be accompanied by EMD of 1% of the amount by DD drawn in favour of the Principal, Govt.Engineering College, Thrissur with an agreement in Kerala Stamp Paper worth Rs.200/-. Details can be had from the Govt.Engineering College Office working hours..

Copy to: D1/1968/17

PRINCIPA1

D/1958./17. F. MO. D/34/17-18.

Data Acquisition System

Detailed Specification:

No. of inputs	Data Acquisition System
Measurement intervals Measurement accuracy Internal memory canacity	10 12 channels
a) Power, Voltage Current	
Alarm Function	±1.0% of Range ±1.0 z
USB port	Required Required

File NO. D, / 1966/17 T-NO. D, /35/17-18.

S.No.	Item with specification	Quantity
1	TMS320F28335 Based DSP Board and JTAG	
	Spec:	6 Nos.
	DSP TMS320F28335 Development board , 15	,
	ADC inputs, 12 channel PWM outputs, Push	
	button switches, LED indicators, on board	
	incremental encoder, DAC outputs,	
	USB connectivity and XDS100 JTAG.	
	with instructions, data manual and	
	representative sample programs	
2	Xilinx Spartan6 Based FPGA Board and	6 Nos
	JTAG.	
<u> </u>	Spec: Xilinx Spartanó FPGA with minimum	
	80 Input/Output lines, Platform flash, LED	
	indications, power supply, JTAG.	
	with instructions, data manual, and	
	representative sample programs	
3	4 Leg, 10 KVA inverter stack for laboratory	3 Nos
	experimental purpose. All rectifiers filters and	
	power supplies are to be in built. Connections	
	brought out to terminals for easy connection	1
	arrangements. Capable of switching up to 25	'
	KHz. Four current sensors in each phase and	
	one voltage sensor. Over current protection	
	and short circuit protection.	
4	dspic 30f2010 based inverter control board for	3 Nos
	three phase induction motor drives with	
	debugger connectivity and with atleast two 10	
	bit DAC outputs	